Supporting Information:

Transistors Formed from a Single Lithography Step Using Information Encoded in Topography

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Design

The schematic diagram of a MOSFET in Figure S1 consists of two aluminum pads, separated by a defined distance. The gate electrode is also aluminum and is separated from the substrate by a thin dielectric (e.g. SiO_2). A bias is applied across the source and drain and the current that flows between the two pads is modulated by the bias applied to the gate. The bias of the gate controls the concentration of charge carriers in the channel (defined as the region of doped silicon connecting the source and drain). We removed the extra silicon surrounding the device (not shown) to eliminate alternative conduction pathways between the source and drain.

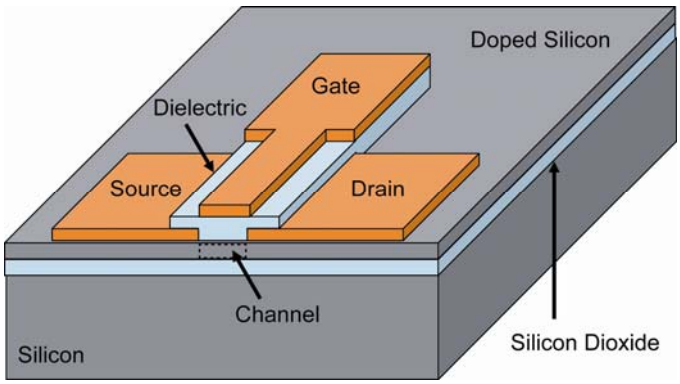

Figure S1. A cut-away schematic of the transistor architecture that we sought to fabricate by shadow evaporation. The source, drain, and gate pads are metal (e.g. Al). The gate pad is separated from the substrate by an insulating dielectric layer (e.g. SiO_2). The substrate is a silicon-on-insulator (SOI) wafer and the insulating layer confines the carriers to the top silicon layer. Carriers conduct through the channel between the source and drain and the current is modulated by the bias applied to the gate.

Resistors

We formed a resistor using an approach similar to that used to form the ohmic connector (Figure 5). The MOSFETs are fabricated by the sequential deposition of metal (conductor) and oxide (dielectric). We therefore sought a material with an intermediate conductivity –the thin, top layer of silicon of the SOI substrate—to form the resistive elements. A wet etch removes all of the exposed silicon during the final step of the process used to fabricate the MOSFETs. We defined the resistive pathways of silicon by depositing oxide (via shadow evaporation) to protect the underlying silicon during the etch step; the silicon that remains under the oxide after etching ultimately defines the resistive element.

We fabricated a resistor ~100 microns long and ~20 microns wide and measured a resistivity of 64 Ω·cm (the listed resistivity of the wafer was 20 Ω·cm). The resistance through the resistor was 300 times greater than that through the channel at zero gate bias. This particular approach to fabrication demonstrates the ability to define structures in a subtractive manner. The shadow deposition defines a passive element (here, oxide) that serves as an etch mask to define structures in the underlying materials during subsequent etch steps.

Figure S2 illustrates an alternate design of a resistive element that can be fabricated on the same substrate as the MOSFET devices and ohmic connectors described in the manuscript (Figures 2-5). An opening in the resist allows the pathway to be illuminated during oxide deposition (i.e., when the substrate is oriented at $\theta = 90°$ and 270°) and shadowed during the metal deposition. During the deposition of the gate oxide, these regions became covered with oxide. The oxide insulates the underlying Si from the

parallel conductive pathways (Figure S2 (c)) such that electrons have to travel through the underlying Si, which is significantly more resistive than the metal. The conductive pathways in Figure S2 can connect adjacent transistors, as demonstrated by the AND device in the manuscript.

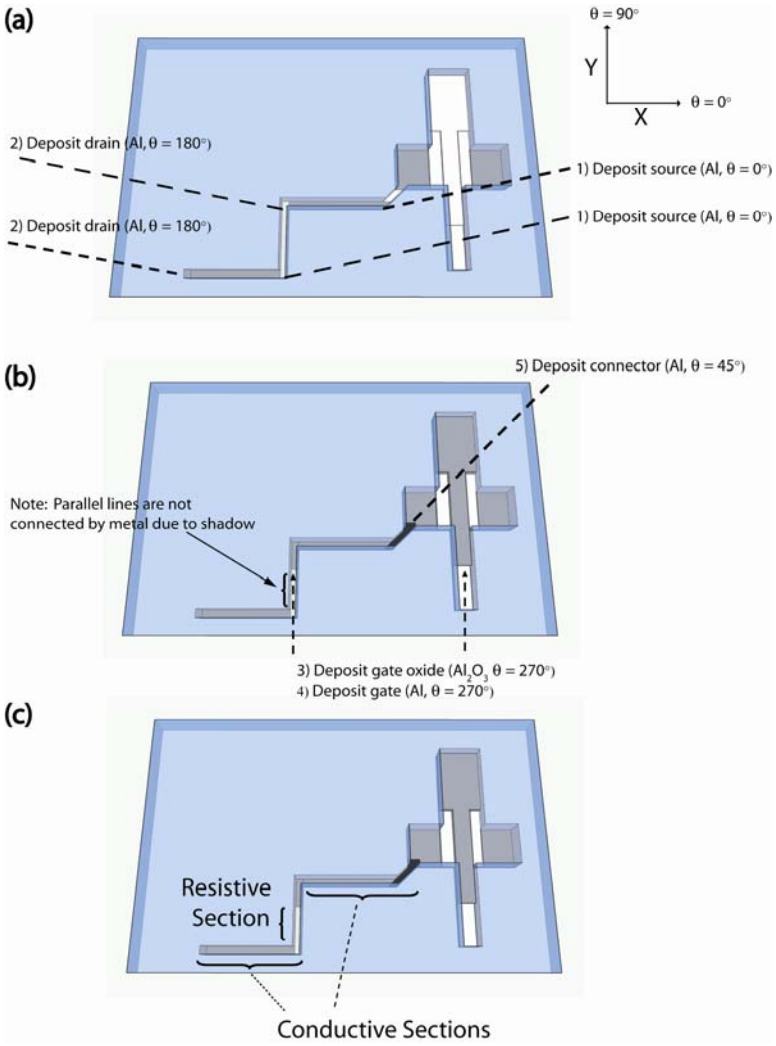

Figure S2. Top-down schematic of a void pattern that produces a resistor while simultaneously producing a transistor. (a) The source and drain depositions are done parallel to the X-axis and simultaneously produce conductive sections that are parallel to the X-axis. (b) The gate oxide is deposited parallel to the Y-axis and also deposits oxide in the "resistive section" because it is parallel to the Y-axis. Deposition of the gate metal (and the 45 degree connector) does not result in metal connecting the two conductive elements; thus, a resistive section (c) is produced between the conductive sections.

Experimental

We used a modified recipe to process SU-8 (Microchem) to improve adhesion to the substrate and to minimize cracking of the resist. We cleaned the substrates (typically, silicon-on-insulator wafer from Ultrasil Corporation) using an oxygen plasma (20 sccm O_2, 80 W, 5 min, Technics Plasma Cleaner).

We coated the substrate with LOR 10B by spin coating (3000 RPM, 60 s) and baked it at 195 °C for 5 min. We then coated the substrate with SU-8 by spin coating (2400 RPM, 30 sec). Profilometry verified the thickness to be ~ 50 microns. We baked the resist on a hot plate by ramping the plate to 75 °C at ~450 °C/hr, baking at 75 °C for 5 min, and then cooling to room temperature. We exposed the resist through a transparency mask (CAS Outputcity) for 11.8 sec at 25 mW/cm^2 (ABM Mask Aligner) and baked the resist on a hot plate at 65 °C for 30 minutes using heating and cooling ramps. We developed the features in SU-8 Developer (Microchem) for 6 min.

To undercut the LOR 10 B, we soaked the wafer in a 1:4 solution of 400K:DI water for 6.5 min, rinsed with DI water, and dried the substrate with nitrogen. We removed any residual polymer using an oxygen plasma (Technics, 60 W, 1 min, 100 mT, 20 sccm O_2) and removed the native oxide using reactive ion etching (30 sccm CF_4, 10 sccm Ar, 70 mT, 100 W, 30 sec). We immediately placed the substrate in an e-beam evaporation chamber. We used e-beam evaporation because it is capable of achieving high rates of deposition (~1 nm/s) and it provides a collimated source of material for deposition; collimation is critical for shadow evaporation.

We deposited 50 nm of Al for the source and drain, ~80 nm of oxide (SiO_2 or Al_2O_3) for the first gate oxide layer, and 80-300 nm of oxide for the second gate oxide layer, and 80 nm of Al for the gate. For the AND gate, we deposited ~50 nm of Al on the connectors. We removed the resist using PG Remover (Microchem) for 60 min at 60 °C, rinsed the substrate with isoproponal, and dried it with nitrogen.

To remove the Si surrounding the device, we placed the substrate in an aqueous solution of tetramethyl ammonium hydroxide (5 wt%), Si (16.5 g/L) and ammonium peroxydisulfate (4 g/L) for 1.5 hr at 80 °C. This formulation selectively etches Si in the presence of SiO_2 and Al (and Al_2O_3); the device itself therefore serves as an etch mask. This etch step improved the performance of the devices (e.g., by confining charge transport to the channel between the source and drain), but caused some overetching and underetching of the Si in some of the devices. A dry etch process would be preferable, but the wet etch process used here was sufficient for proof of principle.

We placed the substrate in a vacuum oven at 80 °C for 12 hours to remove any solvent or moisture on the device before wire bonding with Al. We characterized the devices with a semiconductor parameter analyzer (Agilent 4156C).

Arrays

We typically use 1 x 1" substrates because they are easy to handle during processing. A substrate of this size can accommodate approximately 1600 transistors. Figure S3 contains images of a typical array. Figure S3 (a) is an optical micrograph of the substrate after the oxide deposition. There is some apparent roughness on the surface of the resist primarily due to the contact lithography process. Figure S3 (b) is a scanning electron micrograph of an array of transistors after the lift off step. Based on visual

inspection, approximately 10-20% of these transistors had flaws (e.g., particles) that presumably arose from extensive processing outside of a cleanroom.

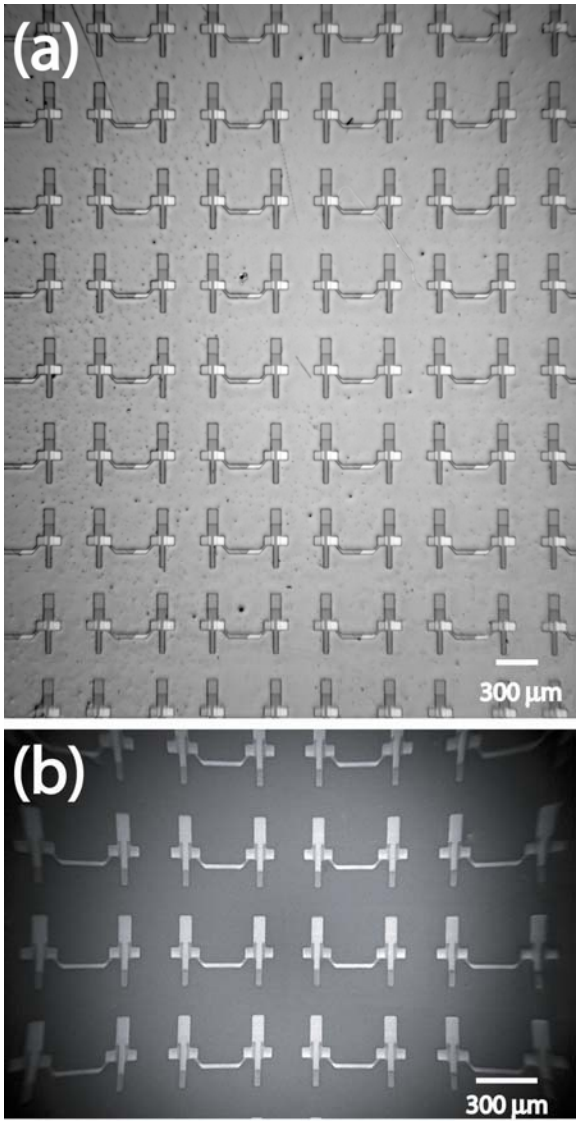

Figure S3. Top-down images of an array of transistors formed by TEMIL. (a) An optical micrograph of the substrate after the oxide deposition. The photoresist appears rough due to the contact lithography step. (b) A scanning electron micrograph of an array of transistors after the lift-off step.

Advantages and Disadvantages of Shadow Evaporation

Alignment and Registration

Conventional transistor fabrication requires the registration of multiple lithographic steps. Lithography is expensive and registration is technically challenging. In contrast, TEMIL only requires one lithographic step and no registration. Shadow evaporation does, however, require alignment of the substrate relative to the depositing beam (θ, Φ). In all of our experiments, we set the angular orientation of the substrate (θ) and the beam orientation relative to the substrate (Φ) crudely by eye with the aid of a protractor. We designed the depositions to have a tolerance of $\Delta\,\Phi \sim 2°$. This tolerance is effectively constant regardless of scaling (see below), whereas conventional registration becomes increasingly difficult with reduced feature size.

Scaling

An appealing characteristic of this method is the way in which the deposited features scale with the geometry of the voids defined in the film of polymer. Simply scaling all of the dimensions of the structured polymer film (X, Y, and Z) by the same factor results in the proportionate scaling of the deposited features without the need to adjust the deposition orientation (Φ, θ). The length of the features defined by shadow evaporation ($X - Z/\tan\Phi$, Figure 1a) depends on the height (Z) and width (X) of the lithographically defined void. These two parameter typically scale proportionally in lithography – that is, smaller features (X) are typically patterned with thinner films (Z) because features with large aspect ratios (Z:X) are difficult to pattern by imprint or photolithography. To some limit, a topographical design for shadow evaporation should

therefore work as well for small as for large features, provided that the ratio of Z:X is constant.

Resolution

There is, of course, a lower limit to the size of features that are practical to fabricate using shadow evaporation. In principle, the resolution of shadow evaporation at small (<100 nm) length scales is limited by several factors, all of which broaden and blur the edge of the illuminated region: (i) imperfect collimation of the evaporation beam; (ii) uncertainty in Φ and θ; (iii) surface migration of the depositing species on the substrate;[1] and iv) irregularities in the topography of the patterned film and the edge of the pattern. The "spread" in Φ due to imperfect collimation should contribute minimally to the resolution limitations since the mean free path in a vacuum of $\sim 1 \times 10^{-6}$ torr (approximately the pressure in our experiments) is ~ 50 m,[2] whereas typical evaporators have source to sample distances less than 0.5 m). There is, however, a small yet predictable spread in Φ since the source (i.e., the crucible liner) is not a perfect point source; we accounted for this approximate one degree deviation during the alignment of the substrate prior to deposition. Substrate vibration (tip / tilt) can alter the orientation Φ, θ, but these effects should also have minimal effect with substrate holders that are designed carefully. Some studies suggest that surface migration—facilitated by the momentum of the depositing material—may alter the deposited geometry from the theoretical line-of-sight value by as much as 7 nm.[3] Despite these limitations, shadows cast over topography have been used to make two electrode junctions with sub-10-nm

gaps.[4-6] Stencil masks, which also cast shadows, have also been used to make 10-nm features.[7]

Deviations from Ideality

The deposited features can deviate from ideality due to (i) the roughness of the lithographically defined edge that defines the shadow, (ii) imperfect initial alignment of the substrate relative to the beam, and (iii) changes in the height of the topography during the deposition. Figure S3 depicts several of these sources of deviation from ideality. In principle, the edge can have roughness in the plane of and perpendicular to the plane of the substrate. Edge roughness perpendicular to the plane should be minimal since films formed by spin-coating are extremely smooth. Edge roughness in the plane of the substrate is akin to the issue of line edge roughness in photolithography; state of the art lithographic features have line edge roughness of ~3 nm.[8] A substrate holder that allows the user to accurately orient the substrate should minimize error associated with poor alignment (in this work, we performed all alignments by naked eye). The height (Z in Figure 1) of the polymeric features increases as material deposits on top of the features; this factor will increase the length of the shadow as a function of deposition time and will only be of significance for thin polymer films.

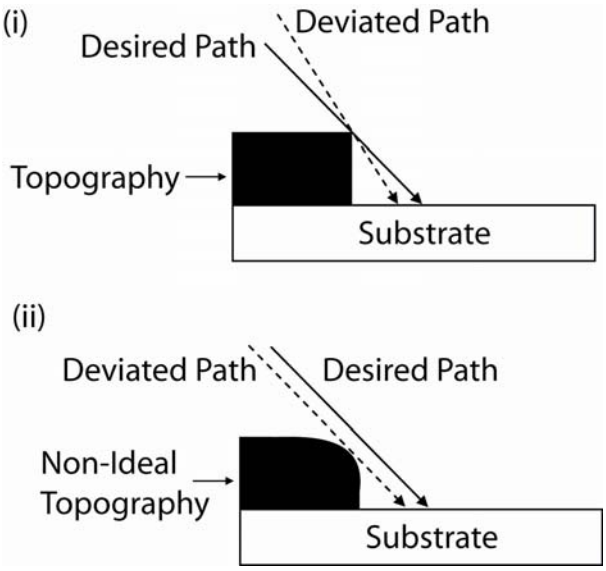

Figure S3. A schematic depiction of potential sources of error during TEMIL. (i) Imperfect collimation or uncertainty in the alignment of the beam relative to the substrate can result in a deviation from the intended beam path. (ii) Imperfections and irregularities in the edge of the topography can result in deviations from the desired beam path.

Another consideration of shadow evaporation is that the orientation of the beam with respect to the substrate varies across the substrate because the source is effectively a point source (in which the emission of evaporated material from the source follows a cosine function[9]), whereas the substrate is effectively a two dimensional plane. This variation can be accounted for with proper layout of the features.[10]

Film Quality

Evaporated films are generally of lower quality (e.g. lower density) than those formed by atomic layer deposition or chemical vapor deposition; in some cases, the quality of the film can be improved by using specialized techniques, such as heating the substrate during deposition.[11] Heating can only be performed within the limits of

stability of the organic photoresist and may deform the photoresist features due to thermal expansion.[12] Alternatively, the thin-film structures deposited by shadow evaporation can be used as an etch mask to define structure in an underlying substrate or film in a subtractive manner; this approach greatly increases the quality and number of materials that can be patterned. We demonstrated this approach to remove the excess silicon of the SOI substrate by using the transistor itself as an etch mask (Figure 2, step 11).

References

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