Transistors Formed from a Single Lithography Step Using Information Encoded in Topography

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This paper describes a strategy for the fabrication of functional electronic components (transistors, capacitors, resistors, conductors, and logic gates but not, at present, inductors) that combines a single layer of lithography with angle-dependent physical vapor deposition; this approach is named topographically encoded microlithography (abbreviated as TEMIL). This strategy extends the simple concept of 'shadow evaporation' to reduce the number and complexity of the steps required to produce isolated devices and arrays of devices, and eliminates the need for registration (the sequential stacking of patterns with correct alignment) entirely. The defining advantage of this strategy is that it extracts information from the 3D topography of features in photoresist, and combines this information with the 3D information from the angle-dependent deposition (the angle and orientation used for deposition from a collimated source of material), to create 'shadowed' and 'illuminated' regions on the underlying substrate. It also takes advantage of the ability of replica molding techniques to produce 3D topography in polymeric resists. A single layer of patterned resist can thus direct the fabrication of a nearly unlimited number of possible shapes, composed of layers of any materials that can be deposited by vapor deposition. The sequential deposition of various shapes (by changing orientation and material source) makes it possible to fabricate complex structures—including interconnected transistors—using a single layer of topography. The complexity of structures that can be fabricated using simple lithographic features distinguishes this procedure from other techniques based on shadow evaporation.

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1. Introduction

This paper describes the fabrication of single transistors (and arrays of transistors) by a process that combines a single level of topography (defined by photolithography or molding, for example) on a substrate with multiple shadow evaporations. We call this technique topographically encoded microlithography (TEMIL). It encodes all the information needed to fabricate a complex structure—such as a transistor—in the topography of patterned polymer. It has the conceptual attraction that it replaces several steps of lithography—each of which require registration—with a single step of patterning and several steps of oriented deposition. Most lithographic techniques (e.g., photolithography, e-beam lithography, and imprint lithography), are generally treated as two-dimensional (2D); that is, even though the lithographically defined features of photoresist have height, it is the shape of the opening in the photoresist in the 2D plane that defines the shape of the pattern on the underlying substrate. Using both the opening and the height of the features (topography) increases significantly the effective complexity of a pattern derived from a single layer of topography. Although the demonstrations in this work involve only a single level of topography, the same principles apply to more complex surfaces.

The progress of microelectronic technology described by Moore's Law has largely been driven by the economics of reductions in the cost per transistor. Advances in photolithography have coupled "cost" and "feature size": that is, "smaller" has, for several decades, also been "less expensive". There are, of course, other ways of reducing cost (especially by reducing reliance on photolithography; hence the active current interest in methods of fabrication based on molding and imprinting[1–4]). Molding, in particular, has the ability to reproduce three-dimensional (3D) features with nanoscale accuracy,[5,6] and imprint lithography can pattern features over large areas rapidly and economically.[4,7–9] The question then becomes, "How does one convert a surface with information encoded in topography into electrical (or optical, or magnetic) function?" Most approaches to this question have transferred patterns directly to the exposed regions of the substrate (i.e., those that are not covered by polymer); the function of the lithographic features is therefore two-dimensional. This paper demonstrates the value of the information coded in the third dimension of a thin, structured polymer film to generate electronic function. The structured film represents an abstraction of the final device—rather than a literal image of the desired structure—because the information is coded in the 3D topography rather than the 2D footprint.

As a demonstration of this method, we used multiple, angle-dependent depositions ("shadow evaporations") over a single layer of lithographically defined features to fabricate single and interconnected transistors (metal-oxide semiconductor field-effect transistors, MOSFETs, interconnected to form an AND gate), and conductive pathways. The architectures of these devices are defined by the topography of the photoresist, and by the orientation of the substrate with respect to the evaporation source; each component of the transistor (source, drain, gate dielectric, gate) is defined by a unique orientation. The composition of the transistor is defined by the choice of evaporated materials. This method produces transistors without any doping, etching, or lithographic alignment steps. In principle, a fully developed process would reduce the time, materials, and complexity of equipment to form a transistor compared to conventional methods (e.g., multi-step lithography).

It is well known that physical obstructions, such as topography or structures suspended over a surface, cast shadows when placed in the path of a collimated deposition source. Shadow deposition through stencil masks has been used to fabricate nanostructures and devices (e.g, nanowires, rings, sensors), but the masks must be registered with the substrate prior to each deposition, the apertures of the stencil reduce in size during deposition, and the method is effectively as two-dimensional as photolithography.[10–18] Structures ("bridges'') suspended across lithographically defined openings have been used to create simple structures by shadow evaporation.[19] This approach alleviates the need for registration, but fabricating these suspended structures is challenging. This approach is used to fabricate small (~0.010 μm^2) metal-insulator-metal tunnel junctions by depositing a metal wire that overlaps an oxidized metal wire.[20–24] The use of this technique to fabricate more complex structures has been limited by its complexity and the inadvertent shadows cast by the suspended structures. Shadow evaporation over the edges of photoresist has been used to deposit simple nanowires (20–30 nm wide) that are smaller in size than the openings in the resist.[19,25–27] A technique called glancing angle deposition (GLAD) has been used to fabricate micro-columnar structures on planar substrates by utilizing the 'shadows' cast by the initial atoms that deposit on the substrate during physical vapor deposition.[28–31] These structures may be useful for optical applications.[32] Shadow evaporation over topography (e.g., metal wires, arrays of self-assembled spheres, the pores of alumina membranes) has also been used previously to form small electrodes,[33–40] arrays of nanotubes,[41] magnetic wires,[42] gradient structures,[43] x-ray masks,[44] imprint molds,[45,46] components for MEMS,[47] single electron devices,[48] molecular junctions,[49] structures that show Coulomb blockades,[50] and simple nanostructures[51–53]. TEMIL can fabricate complex (multilayer, functional, interconnected) microsystems without the issue of registration involved in the use of stencil masks, and without the complexities associated with suspended bridge structures. The method described here suggests a different approach to the use of topography to encode information useful in the fabrication of functional, interconnected micro- and nanosystems.

2. TEMIL

As a demonstration of TEMIL, we fabricated individual MOSFETs (in arrays containing ~1600 devices), and a pair of transistors connected to form an AND gate with resistive and conductive pathways, all using a single layer of photolithography. **Figure 1** illustrates how multiple shapes can be fabricated on a substrate from a single simple lithographic feature (e.g., one involving only a single layer of

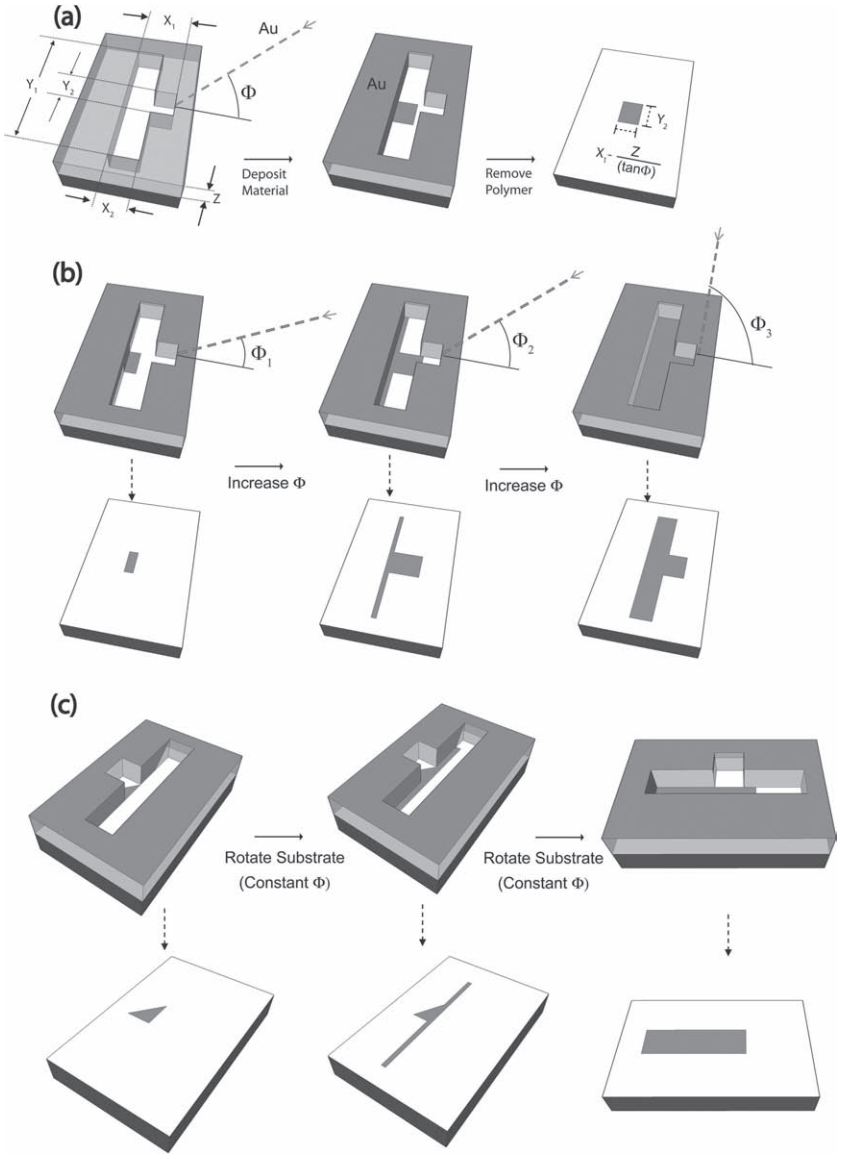

Figure 1. Conceptualization of TEMIL. Multiple shapes can be formed with one lithographic feature. (a) A rectangular-prism shaped relief structure is defined on a substrate. The angle Φ defines the orientation of the vectorial path of depositing gold atoms with respect to the substrate (or the X-Y plane). The angle θ defines the angular orientation of the substrate within the X-Y plane. In this particular example, the deposition path is parallel to the X-Z plane. The photoresist casts a shadow of length $Z/\tan(\Phi)$ onto the base of the opening; thus, material deposits over a length $X_1 - Z/\tan(\Phi)$. The deposited material has a width of Y_2 and is effectively independent of dimension Y_1. (b) Increasing the angle Φ, while keeping the other parameters constant, decreases the length of the cast shadow and the resulting structures vary accordingly (the features are depicted before and after removal of the polymer). (c) Varying the orientation of the rotational orientation of the substrate, θ, while keeping the other parameters constant, determines the direction that the shadow is cast.

topography) by using TEMIL. Figure 1a depicts an opening patterned into a film (e.g., a "resist", which could either be a photoresist or a molded polymer) of thickness Z. A collimated beam of evaporating metal (gold, as depicted) is aligned parallel to dimension X and oriented at an angle Φ relative to the surface of the resist. Although the opening in the film is a polygon with eight sides, the material deposited on the substrate is a square. A square forms because shadow evaporation is a "line-of-sight" technique[54] in which a collimated beam deposits material on a substrate in a pattern determined by (i) the topography on the substrate and (ii) the orientation of the substrate with respect to the source of material. Shadow evaporation creates simultaneously "shadowed" and "illuminated" regions on the portions of the substrate not covered by polymer. In Figure 1a, Au deposits on only a fraction of the exposed substrate; we refer to this portion as "illuminated" and the remaining portion as "shadowed". In general, the length of a shadow cast by a beam over topography is $Z/\tan(\Phi)$, in which Z is the height of the resist and Φ is the angle between the beam and the plane of the resist. In Figure 1a, the shadow is longer than X_2 but shorter than X_1. As a result, the substrate is only illuminated in region Y_2 (and the pattern formed is completely independent of dimension Y_1). The deposited material therefore has in-plane dimensions Y_2 and $X_1 - Z/\tan(\Phi)$.

Figure 1b illustrates how the shape of the material deposited on the substrate changes with the angle Φ of the beam relative to the resist. As Φ increases (with all other variables remaining constant), the length of the shadowed region decreases and the illuminated region increases. Each change in Φ produces a shape with unique dimensions. In some cases, the change in the shape arising from these changes can be dramatic. For example, in Figure 1b, the shape changes from a rectangle to a square to a polygon. When Φ reaches 90°, the beam is perpendicular to the substrate and the shape of the illuminated region on the substrate replicates the shape of the opening; this condition is used during conventional patterning.

Figure 1c illustrates how the shape of the illuminated region is affected by varying the angular orientation (θ) of the substrate (i.e., by rotating the substrate within the X-Y plane) while keeping the beam orientation (Φ) constant. The angular orientation θ dictates the region of the substrate that is shadowed for a given beam angle Φ, and changing θ can also change entirely the pattern of deposited material (from a triangle to a rectangle in Figure 1c). Complex structures, such as a MOSFET, can be fabricated by combining multiple, sequential depositions of various materials, each at a unique orientation. Using this method, each functional layer of the device can be deposited independently, using a single level of topography.

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3. Experimental Design

We fabricated MOSFETs using only one layer of lithography, and multiple shadow evaporation steps, to demonstrate the utility of TEMIL for fabrication. MOSFETs—ubiquitous in modern integrated circuits—are complex, multicomponent structures. MOSFETs typically contain regions directly under the source and drain pads that are doped to levels that give conductivities greater than that in the channel (often the inherent doping of the substrate). We did not incorporate any doping steps beyond the inherent doping of the wafer. This approach has been used by others to fabricate back-gated transistors.[55] We used a "depletion mode" MOSFET design (see supplemental Figure S1) in which charge carriers are depleted from the channel by a bias applied to the gate.[56] This approach requires the use of silicon-on-insulator (SOI) wafers that have a thin (<0.2 μm thick) silicon layer, which confines the depth of the channel through which the charge carriers conduct.

In this demonstration, we fabricated features on the 50–100 μm length scale because these dimensions are (i) easy to fabricate using commonly available lithographic tools (contact lithography) and (ii) simple to characterize electrically because the source, drain, and gate pads can be addressed directly using a wire bonder (wire bonds are ~50 μm in diameter). We designed the layout of the photoresist features such that each transistor could be addressed electrically with a wire bonder without concern of overlapping with neighboring devices (~200 μm separated the transistors). The design was therefore intended to facilitate addressing rather than maximizing feature density. We typically fabricated arrays of ~1600 transistors on each substrate (1 × 1"). The supporting information contains an image of an array of transistors formed using TEMIL. To show that more than one transistor formed by shadow evaporation could be linked together using features in the same single layer of patterned resist, we fabricated AND devices by connecting the source and drain pads of adjacent transistors with an electrically conductive pathway.

4. Experimental

The supplemental information contains experimental details; a brief summary follows. Onto a 1 × 1" piece of SOI wafer (~0.2 μm Si on ~1 μm oxide), we spin-coated a thin film (~1 μm) of poly(methylglutarimide) (LOR 10 B, Microchem). On top of this film, we patterned features in a 50-μm-thick film of SU-8 2025 (Microchem) using contact photolithography. A typical pattern was a 40 × 40 array of transistors. The target height of the features (i.e., the thickness of the SU-8 film) ultimately depended on the desired angle of evaporation and the dimensions of the patterned features. The poly(methylglutarimide) was necessary for the lift-off process, because SU-8 is an insoluble, highly crosslinked polymer that has excellent adhesion to silicon wafers. Bilayer lithography schemes are used routinely for other patterning techniques such photolithography,[57] imprint lithography,[8] and self-assembled block copolymer lithography[58], so this approach is not limited to SU-8, and should be applicable to patterning layers made of other polymers, ceramics (e.g., thick SiO_2 or other metal oxides), or even metals.

Figure 2 outlines the sequence of steps involved in the fabrication of a MOSFET using one layer of lithography. The orientation of the substrate is critical during fabrication. We define the coordinate axes (X, Y, Z) in Figure 2 such that the Y-axis is always perpendicular to the vector path of the beam of depositing material and the Z-axis is always perpendicular to the substrate surface. Changes in the orientation of the beam vector, Φ, therefore occur in the X-Z plane. Prior to each deposition, the substrate is rotated to a specific orientation θ within the X-Y plane. We arbitrarily define $\theta = 0°$ as the orientation of the substrate depicted in the first processing step in Figure 2. We typically deposited the gate dielectric from two opposing angles ($\theta = 90°$ and 270°) to prevent electrical shorting between the gate metal and the substrate.

Following the final deposition, immersion of the substrate in acetone lifted-off the resist. A subsequent immersion in an etching solution of tetramethyl ammonium hydroxide (TMAH), dissolved Si, and ammonium peroxydisulfate ($(NH_4)_2S_2O_8$) removed selectively the Si surrounding the features of the transistor,[59,60] thereby eliminating any conductive pathways around the periphery of the device. This formulation etches Si preferentially over silicon oxide, aluminum oxide, and aluminum, allowing the device itself to be used as an etch mask and the oxide layer of the SOI wafer to be used as an etch stop. An optical micrograph of a completed device is shown in **Figure 3**. We made individual electrical contacts from the source, drain, and gate of each MOSFET using an aluminum wire bonder and characterized the device electrically using a semiconductor parameter analyzer.

5. Results and Discussion

MOSFET: **Figure 4** shows the traces of current vs. applied voltage (I–V) between the drain and source for various gate voltages, and shows its output characteristics. We achieved an on:off ratio (defined as the ratio of current at $V_G = 0$ V and $V_G = -40$ V at $V_{DS} = 1$ V) of 4.5×10^2. We measured the leakage current through the gate to the drain at $V_G = 40$ ($V_{DS} = 0$) to be four orders of magnitude lower than that through the channel for $V_{DS} = 1$ V ($V_G = 0$ V); this result suggests that the gate dielectric electrically insulated the gate from the substrate. Both the transconductance and gate leakage could presumably be improved by optimizing the properties of the gate dielectric. The substrates typically contained ~1600 transistors. Based on visual inspection, approximately 20% of these transistors had obvious flaws (e.g., particles) that presumably arose from extensive processing outside of a cleanroom.

AND Gate: TEMIL can also be used to fabricate interconnected MOSFETs using a single layer of lithography. We fabricated two connected devices using the same process that was used for the fabrication of the MOSFETs. As a proof of principle, we fabricated an AND gate that incorporates the same basic MOSFET design shown in Figure 2 but with

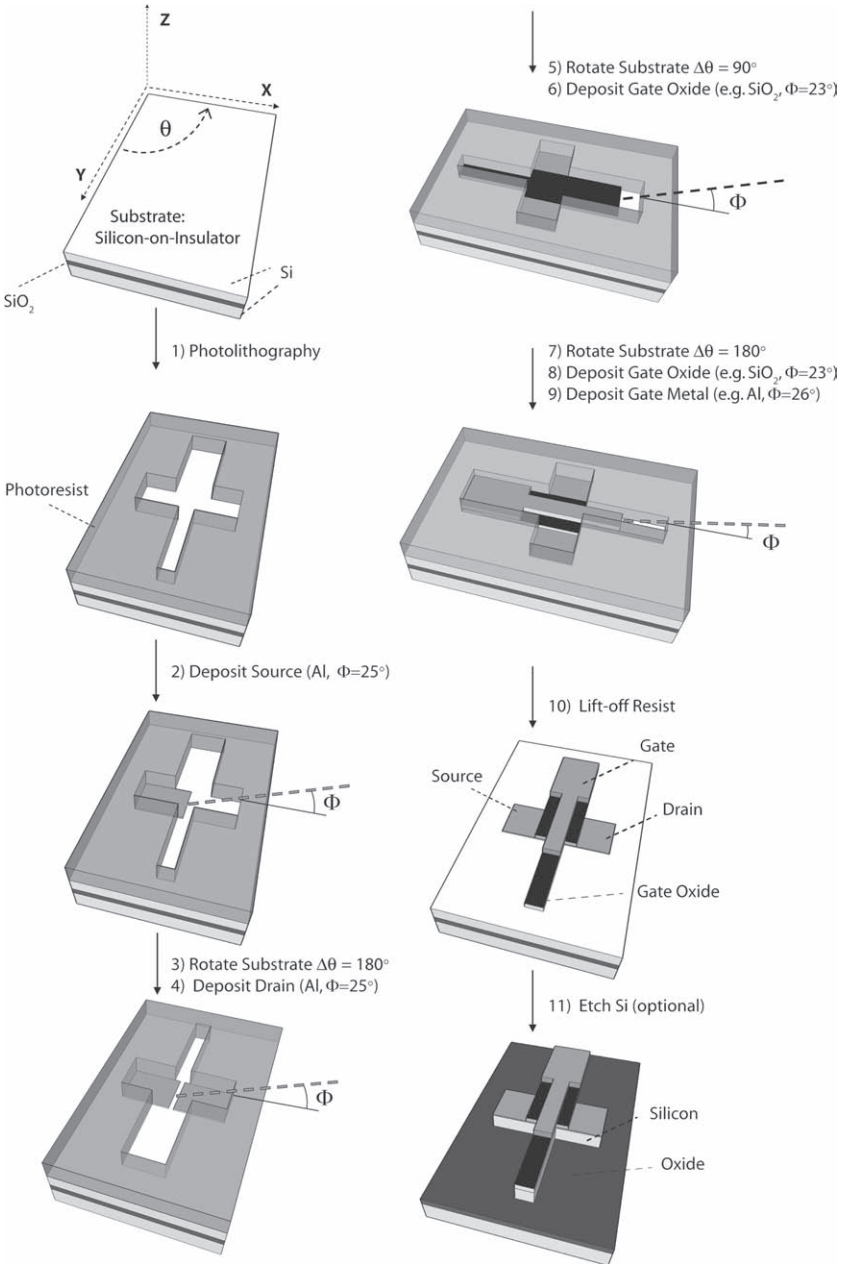

Figure 2. Schematic of the formation of a transistor by shadow evaporation on a silicon-on-insulator substrate. (i) We first defined features by photolithography. (ii) We evaporated aluminum to form the source pad. We oriented the substrate such that the evaporating material would follow the path denoted by the dotted arrows ($\theta = 0°$). The topographical resist features cast shadows such that the metal only reaches the substrate in a defined region. (iii) To define the drain, we rotated the sample 180° in the plane of the substrate and evaporated aluminum. (iv) We then rotated the sample 90° and evaporated oxide to electrically insulate the source and drain pads from the gate. (v) We rotated the sample 180° and evaporated oxide to provide more electrical insulation, and, (vi) Without changing the orientation, we evaporated aluminum to define the gate electrode directly on top of the oxide dielectric. We lifted-off the resist features using solvent, leaving behind a MOSFET architecture. The surrounding silicon could be selectively etched to improve the performance of the device by confining electron transport to regions under the deposited features.

an electrically conductive connector between the drain pad of one device and the source pad of the adjacent device. In principle, this approach could be adapted to connect a large number of transistors; developing design rules for such systems will require integrating materials and topography with circuit design. **Figure 5**a is a circuit diagram for the AND gate fabricated here.

Figure 5b outlines the procedure used to fabricate the electrical connector (a continuous wire) between adjacent transistors. The connector consists of three sections that are fabricated over the course of four depositions. One section is deposited with metal concurrently with the source and drain depositions ($\theta = 0°$ and 180°) and the other sections consist of two symmetrical, shorter pathways that are deposited with metal at an incident angle of $\Phi = 16°$ and orientations of $\theta = 45°$ and 135°. These depositions of metal link the conductive sections to the source and drain pads of adjacent transistors without inadvertently depositing metal onto regions of the substrate that could alter the operation of the individual transistors. All of the sections of the connector are shadowed during deposition of the gate dielectric (i.e., when the substrate is oriented at $\theta = 90°$ and 270°) to ensure they are electrically continuous. (The Supporting Information includes a description of the fabrication of a resistor—three hundred times more resistive than the channel at zero gate bias—by changing the geometry of the connector such that it intentionally incorporates insulating materials.) The conductivity of the metallic connector is $2.4 \times 10^7\ \Omega^{-1}\ m^{-1}$ (the value of bulk aluminum is $3.7 \times 10^7\ \Omega^{-1}\ m^{-1}$). The additional resistance is expected since the substrate is exposed to atmosphere between depositions. Our experimental configuration required us to open the evaporation chamber to orient the substrate between depositions; the exposure to oxygen likely resulted in imperfect junctions between the individual sections of the connector.

Figure 5c is an optical micrograph of a completed AND gate. The measured current from the input and output (Figure 5a) as a function of voltage applied to each gate is listed in **Table I**. This result demonstrates AND gate functionality, although practical use would require improved performance for the (1,0) state.

6. Advantages and Limitations of TEMIL

Conventional transistor fabrication requires the registration of multiple lithographic steps. Hewlett-Packard is developing a process called self-aligned imprint lithography (SAIL) in which arrays of transistors may be formed

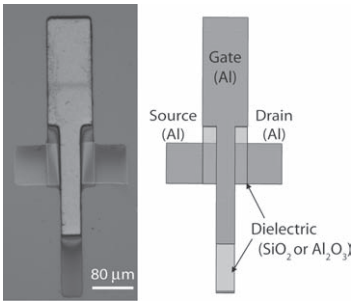

Figure 3. (left) Optical micrograph of a field effect transistor formed by combining one layer of lithography and shadow evaporation. This image depicts one of an array of 1600 similar devices. (right) A schematic illustration to clarify the features depicted in the micrograph.

without the need for registration by using a single layer of patterning.[61] SAIL uses imprint lithography to create a pattern with multiple levels of topography on top of a planar, multi-layer film stack. The imprinted polymer and the underlying stack of films are alternatively etched, leaving behind the components of a transistor. The SAIL process requires fine control over the etching steps. TEMIL also requires only one lithographic step and no registration, but it does require a collimated beam for metal deposition, and alignment of the substrate relative to the beam (θ, Φ). In all of our experiments, we set the angular orientation of the substrate (θ) and the beam orientation relative to the substrate (Φ) crudely, by eye, with the aid of a protractor. We designed the depositions to have a tolerance of $\Delta\,\Phi \sim 2°$. This tolerance is effectively constant regardless of feature scaling, whereas conventional registration becomes increasingly difficult with reduced feature size. Simply scaling all of the dimensions of the structured polymer film (X, Y, and Z) by the same factor results in the proportionate scaling of the deposited features without the need to adjust the deposition orientation (Φ, θ). To some limit, a topographical design for shadow evaporation should

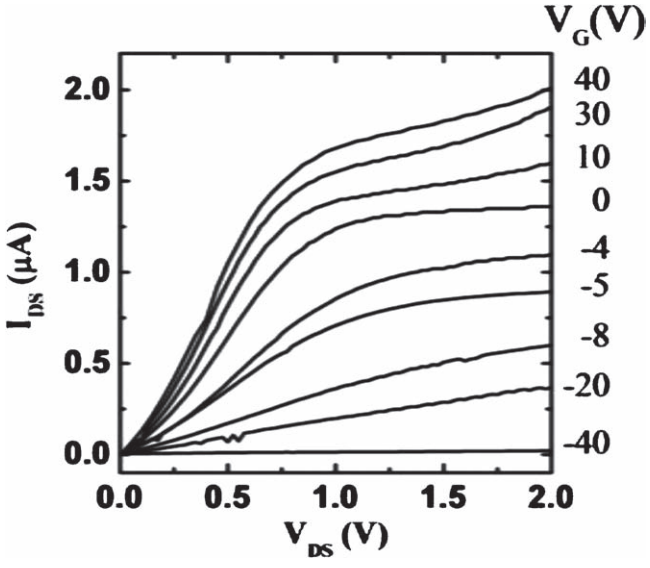

Figure 4. Electrical characterization of a MOSFET formed by shadow evaporation. Current, I_{DS} (μA) between the drain and source as a function of drain-source bias (V_{DS}) for various gate voltages.

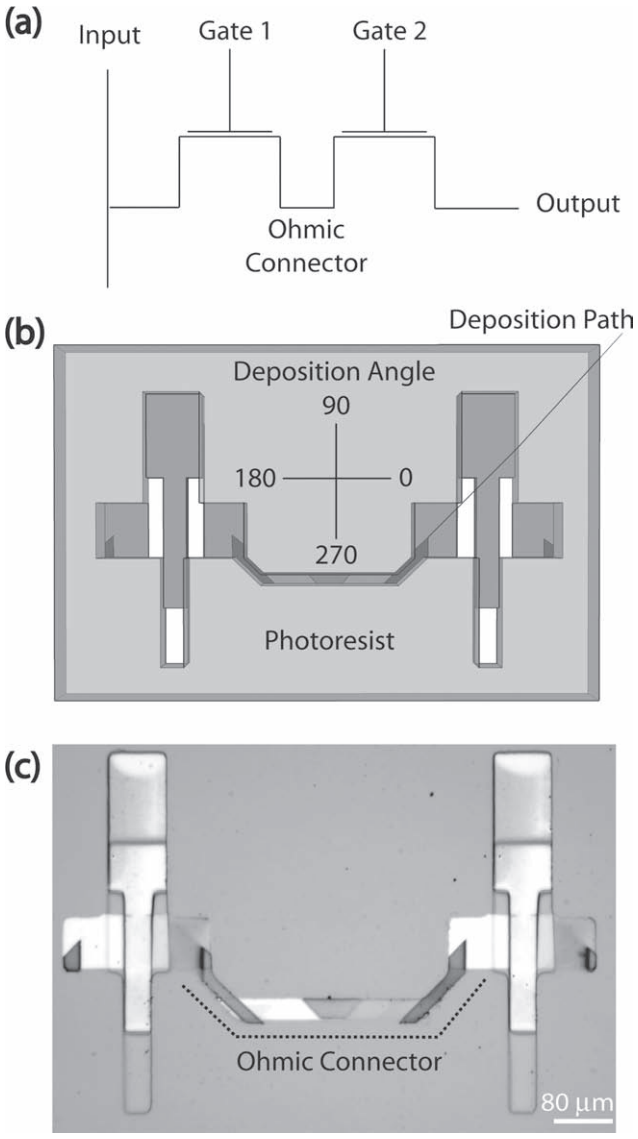

Figure 5. One layer of lithography and shadow evaporation produced an AND logic device by connecting two transistors in series. (a) A circuit diagram of the device. (b) Schematic illustration depicting the way by which a drain pad from one transistor connects to the source of an adjacent transistor. The section of the ohmic connector that is parallel to the source and drain is deposited during the evaporation of the source and drains. The remaining two sections of the connectors are formed by two separate evaporations ($\theta = 45°$, as depicted by line labeled "deposition path" and $\theta = 135°$). (c) A top-down optical micrograph of two transistors with an ohmic connection.

therefore work as well for small as for large features, provided that the features are proportional.

There is, of course, a lower limit to the size of features that are practical to fabricate using shadow evaporation. In principle, the resolution of shadow evaporation at small (<100 nm) length scales is limited by several factors, all of which broaden and blur the edge of the illuminated region: (i) imperfect collimation of the evaporation beam; (ii) uncertainty in Φ and θ; (iii) surface migration of the depositing species on the substrate;[62] (iv) irregularities in the topography of the patterned film and the edge of the pattern; and (v) change in the

Table I. Truth Table for an AND Device (for V_{DS} = 2 V).

Truth Table			Conditions		
Input 1	Input 2	Output	V_{G1}(V)	V_{G2}(V)	I_{DS} (μA)
1	1	1	0	0	2.2
1	0	0	0	−10	0.9
0	1	0	−10	0	0.2
0	0	0	−10	−10	0.2

topography of the shadowing edge as deposition proceeds. These factors are discussed in the supporting information. Despite these limitations, we believe TEMIL can be scaled down to form smaller structures based on previous studies using shadow evaporation. For example, shadows cast over topography have been used to make two electrode junctions with sub-10-nm gaps.[33,36,37] Shadow evaporation has also been used (in conjunction with etching) to make trenches as narrow as 10 nm for the fabrication of asymmetric tunneling transistors by shadow depositing chromium over lithographic features 40 nm tall.[45] Wang et al. studied the effects of variation in the height of the lithographic features and variability of the deposition angle on the desired shadow length.[45] Their experimental results show that the deviation of the shadow from that expected was less than 3 nm for shadows ranging from 10-25 nm in length. These results suggest that the practical limits of shadow evaporation restrict simple features (e.g., gaps, wires) to lengths greater than 10 nm.

We discuss other advantages, limitations, and considerations of TEMIL in the Supporting Information.

7. Conclusions

Topographically encoded microlithography (TEMIL) is an integrated strategy for fabricating microscale devices combining a single lithographic step with multiple shadow evaporations. The current level of demonstration of this methodology is limited to simple components: a MOSFET, an AND gate (two connected MOSFETS), a capacitor (i.e., the gate of the transistor), and a conducting wire with several angles and connections. We have, however, fabricated ~1600 of these components in parallel. The process is scalable, applicable to a wide variety of devices and materials, and compatible with any patterning technique that produces topography (photolithography, soft lithography,[63] step-and-flash imprint lithography,[1] imprint lithography,[3] nanoskiving,[64] anisotropic etching,[65] and block copolymer lithography[66]).

Conventional multi-layer photolithography requires registration (the sequential stacking of patterns with correct alignment) and has poor tolerance for lateral drift (i.e., the deviation from the designed spacing between features on a single level of lithography). Lateral drift is particularly problematic for aligning patterns on dimensionally unstable substrates (e.g., polymeric substrates for flexible electronics), which can result in 100 μm of misalignment over a distance of 1 cm.[61] Soft molding techniques (e.g., soft lithography), which are attractive because of their low cost and high resolution,[5,6] are particularly subject to lateral drift because of the softness of the stamp; Step-and-Flash Lithography (SFIL) developed by Willson combines many of the desirable features of both photolithography and soft lithography. By encoding the information required for fabrication in the topography of a single layer of polymer, TEMIL has the potential to eliminate multiple steps of lithography and pattern registration; it may also be tolerant of the lateral drift that limits soft lithographic techniques.

TEMIL has the ability to accommodate a wide variety of materials. The "illuminated" region created by shadow evaporation can be used directly as a feature (as demonstrated here), or can be used to form a mask to protect the underlying substrate while the "shadowed" region is removed by etching. In our hands, the throughput has been limited by the requirements of manual changes of evaporation sources and manual setting of angles, but the efficiency and versatility of the process could be improved easily by using multiple beams simultaneously or sequentially from different values of Φ and θ using an automated deposition chamber. More importantly, hierarchical resist structures (i.e., structures with two or more heights), would cast shadows of differing lengths depending on the height of each structure; using 3D shadow masks would provide another variable that can be used to alter the geometry of the deposited structure.

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