Using soft lithography to fabricate GaAs/AlGaAs heterostructure field effect transistors

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This letter describes the fabrication of functional GaAs/AlGaAs field effect transistors using micromolding in capillaries—a representative soft lithographic technique. The fabrication process involved three soft lithographic steps and two registration steps. Room temperature characteristics of these transistors resemble those of field effect transistors fabricated by photolithography. The fabrication of functional microelectronic devices using multilayer soft lithography establishes the compatibility of these techniques with the processing methods used in device fabrication, and opens the door for their development as a technique in this area. © *1997 American Institute of Physics.* [S0003-6951(97)03840-0]

Soft lithography—a set of techniques for nonphotolithographic pattern transfer based on contact printing and polymer molding—is now established as an alternative to photolithography in microfabrication.[1-4] While it has been demonstrated that soft lithography has obvious applications in optical[5-7] and microanalytical systems,[8] its potential for application to microelectronic devices remains to be established. Fabrication of such devices requires high reproducibility in pattern transfer, accurate registration between layers, low distortion of the elastomeric molds, and little surface contamination or damage during processing. The objective of the work reported here is to begin to address these issues by using soft lithographic processes to fabricate simple, electrically functional devices, and by establishing the characteristics of these processes.

In this letter we describe the fabrication of field effect transistors (FETs) on a GaAs/AlGaAs heterostructure using a representative soft lithographic technique: micromolding in capillaries (MIMIC).[2] The fabrication process required three molding steps and two registration steps. The FETs have an overall size of 1 mm×0.55 mm with gate length (L) and gate width (Z) both ranging from about 20 to 50 μm. Their characteristics are similar to those of FETs fabricated using conventional photolithographic techniques. These dimensions are not lower limits; we have made simple test structures with dimensions down to 30 nm by soft lithography.[9,10] Rather, these FETs establish that soft lithography is compatible with multilayer fabrication of functional microelectronic devices, and set a benchmark against which to measure further development in this area.

Figure 1 shows the schematic FET structure. The FET was made on a molecular beam epitaxially (MBE)-grown GaAs/AlGaAs heterostructure. Figure 1(a) is a cross sectional view of the wafer, composed of GaAs, $Al_{0.3}Ga_{0.7}As$, and a Si δ-doped layer $n=3.8\times10^{12}$ cm^{-2} 400 Å from the interface. The two-dimensional electron gas (2DEG) is located 1500 Å below the surface. At room temperature, the measured 2DEG density and mobility were 3.9×10^{11} cm^{-2} and 4.0×10^{3} cm^2/V s. In Fig. 1(b) the source and drain are AuNiGe ohmic contacts, the channel is defined by a mesa etch, and the gate is a Cr/Au Schottky contact.

Figure 2 illustrates the process used to fabricate the FET. We used MIMIC in all three fabrication steps. In MIMIC, an elastomeric mold with interconnected recessed regions is put in conformal contact with the substrate. Continuous channels are formed by the recessed regions on the mold and the substrate. A liquid prepolymer is applied to the open ends of the channels and fills the channels automatically by capillarity. The prepolymer is cured either thermally or by long wavelength ultraviolet (UV) light, and the mold is then removed. The elastomeric molds (or stamps) were made by casting polydimethylsiloxane (PDMS, Sylgard 184, Dow-Corning, $A:B=1:15$) on masters generated by a rapid prototyping technique based on patterns printed using a high resolution

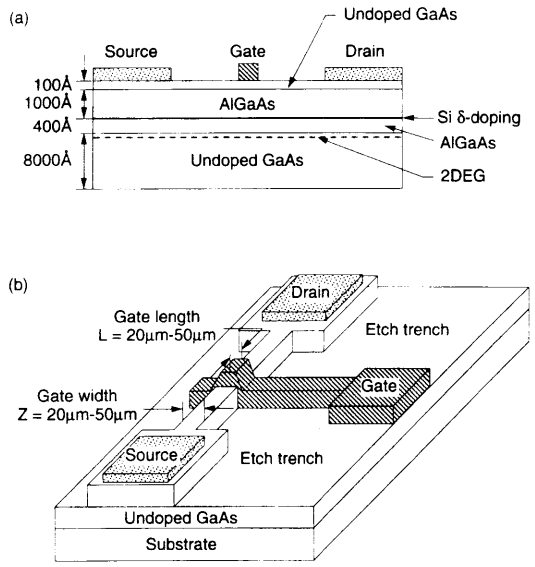

FIG. 1. (a) Schematic cross sectional view of the field effect transistor (FET) to show the growth profile of the GaAs/AlGaAs material. (b) Schematic diagram of GaAs/AlGaAs heterostructure FET.

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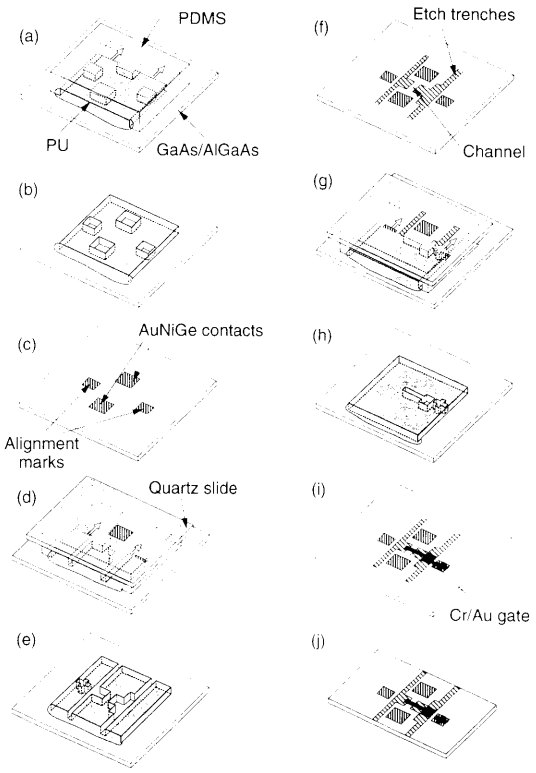

FIG. 2. Schematic illustration of the procedure for FET fabrication. (a) First MIMIC using polyurethane (PU) to define the ohmic contacts and alignment marks. (b) Cure PU, peel off the first PDMS mold, and remove the PU underlayer using O_2 RIE. (c) Evaporate AuNiGe, lift off PU, and anneal to form the ohmic contacts for the source and drain. (d) Register, second MIMIC to define etch trenches. (e) Cure PU, peel off the second PDMS mold, and remove the underlayer using O_2 RIE. (f) Etch in citric acid and hydrogen peroxide solution to remove the 2DEG in the etch trenches. (g) Register, third MIMIC to define the gate. (h) Cure PU, peel off the third PDMS mold, and remove the underlayer using O_2 RIE. (i) Evaporate Cr/Au and lift off PU to form the gate. (j) Cleave two ends to remove the 2DEG in these regions.

image-setting system.[11] The thickness of the PDMS molds used in FET fabrication was typically ~1 mm while the relief structures had 10 μm steps. As shown in Figs. 2(a), 2(d), and 2(g), the recessed regions on the molds were interconnected and had open ends. PDMS is a good choice for the mold material because it wets the sample surface and because it is transparent to the UV light used to cure the prepolymer. The transmission coefficient of a 1-mm-thick PDMS block was 92% at $\lambda = 365$ nm. Samples were cleaned in trichloroethylene, acetone, and methanol before each application of the PDMS mold.

Figures 2(a)–2(c) describe the first molding step: the fabrication of ohmic contacts. The ohmic contacts, source and drain, were 200 μm$\times$200 μm squares separated by 150 μm. Two alignment marks of size 150 μm$\times$150 μm were also defined in the first step for aligning the etch trenches and the gate. The prepolymer, polyurethane (PU) NOA 73 (Norland Products), had a low viscosity (η=140 cps). PU required about 20 min to fill a 6-mm-long channel [Fig. 2(a)] and was cured by exposure to a 450 W UV lamp (Canrad–Hanovia Immersion Lamp, Model 7825-34) for 1 h. The PDMS mold was then removed [Fig. 2(b)]. Often a thin layer of PU (<0.1 μm) diffused into the recessed regions on the sample; this layer was removed using an O_2 reactive ion etch

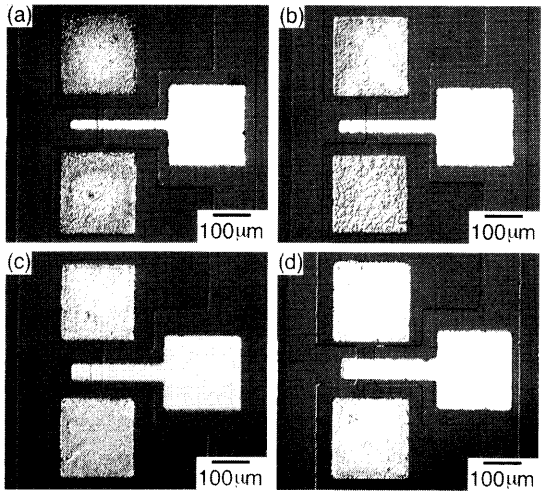

FIG. 3. Micrographs of FETs with various gate lengths L and gate widths Z fabricated by soft lithography. (a) $L = 26$ μm and $Z = 16$ μm; (b) $L = 34$ μm and $Z = 30$ μm; (c) $L = 44$ μm and $Z = 32$ μm; (d) $L = 52$ μm and $Z = 47$ μm.

(RIE).[3] AuNiGe contacts were then deposited by thermal evaporation, the PU was lifted off in methylene chloride, and the contacts were thermally annealed to make ohmic contact to the 2DEG.

Figures 2(d)–2(f) outline the second molding step: making etch trenches to form the channel. Registration of the mesa etch layer to the source and drain contacts was accomplished using a Karl Suss Aligner. The mold was mounted on the aligner by placing its flat surface on a quartz slide [Fig. 2(d)] which, in turn, was mounted on the mask holder of the Karl Suss. Fine registration was achieved by aligning a cross on the second mold with the left square on the sample. Once the mold and the sample were well aligned, they were carefully brought into contact. The PDMS stayed in contact with the sample as a result of Van der Waals interactions. We then moved the mold and the sample from the mask holder and used the same MIMIC procedure as that used for the fabrication of ohmic contacts to obtain the PU structure shown in Fig. 2(e). Chemical etching in 10:1 solution of 50% citric acid and 30% hydrogen peroxide etched away 1800 Å GaAs/AlGaAs to define the channel [Fig. 2(f)].

Figures 2(g)–2(i) describe the third molding step: fabricating the gate. The registration was achieved by aligning the cross on the third mold with the right square on the sample. Due to the elastomeric nature of the mold, it could reliably transfer the pattern even over nonplanar surfaces. We deposited 200 A of Cr and 3000 A of Au by thermal evaporation and lifted off the PU to form the gate. Finally, as shown in Fig. 2(j), the two ends of the sample were cleaved to remove the 2DEG in these regions.

Figure 3 shows representative images of the FETs fabricated by MIMIC. The surfaces of the source and drain were rough as a result of thermal annealing. Both the edge roughness (~2 μm) and the resolution (~10 μm) of these FET structures were determined by the masters. The values for L and Z shown in the figure caption were measured from the micrographs of the FETs. A typical sample with patterned area of 40 mm^2 had about 40 FETs. The number of FETs that could be fabricated at one time was limited by the usable

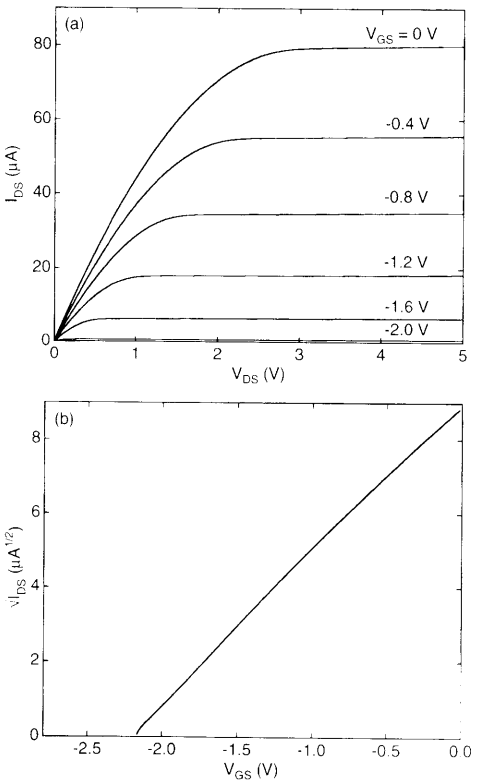

FIG. 4. Performance of a representative FET fabricated by soft lithography. The FET has $L=30$ μm and $Z=21\mu$m. (a) Drain-source characteristics. (b) Transfer characteristics measured at $V_{DS}=4$ V.

area of the strip heater (~40 mm^2) used for annealing. The registration was within 12 μm over a 40 mm^2 area. The main factors that affected registration were the distortion and the variation in thickness of the elastomeric mold. We have also noticed that local sagging of the PDMS mold could occur during registration when one side of the PDMS mold was significantly thicker than the other, $\Delta h \sim 100$ μm. The sagging could however be minimized with special care in bringing the mold and the sample into contact. The first MIMIC step typically had a yield of >98%. The defects arose from regions near the open ends of the PDMS mold. The subsequent MIMIC steps had a yield of ~95%. The additional defects came from local sagging of the PDMS molds associated with the variation in the thickness of the PDMS molds.

Figure 4 shows the measured dc performance of a representative FET with $L=30$ μm and $Z=21\mu$m at room temperature. Figure 4(a) shows the drain-source current I_{DS} versus drain-source voltage V_{DS} characteristics of this FET for a series of gate voltages. These $I_{DS}-V_{DS}$ characteristics were similar to those of FETs fabricated using conventional photolithographic techniques.[12] The channel resistance at $V_{GS}=0$ was $R_{channel}=17.5$ kΩ, the transconductance at $I_{DS}=80$ mA was $g_{m0}=63$ μS, and the breakdown voltage of the FET was $BV_{DS0}=100$ V. The transfer characteristics were measured at $V_{DS}=4$ V, and are shown in Fig. 4(b). As expected, $\sqrt{I_{DS}}$ varies linearly with V_{GS}, similar to that of a heterostructure FET.[12] The pinch-off voltage was determined from the transfer characteristics, and was $V_p=2.2$ V. These characteristics resemble the corresponding values for the heterostructure FETs of similar dimensions fabricated by photolithography.[13]

The final yield of functional FETs fabricated by MIMIC was approximately 70%. In order to check the reproducibility of the performance of these FETs, we compared the characteristics of nine functional FETs, chosen randomly from three samples. Their characteristics scaled with their dimensions. The resistance between the source and drain was $R_{DS}Z=0.42\pm0.05$ Ωm. The scaled transconductance was $g_mL/Z=91\pm14$ μS measured at $I_D=40$ μA. The pinch-off voltage was $V_p=1.6\pm0.6$ V. Disfunctional FETs often showed either poor ohmic contacts or broken gates, associated with incomplete removal of thin polymer underlayers between the deposited metal film and the GaAs/AlGaAs substrate. We believe that these defects can be minimized in the future by optimizing the RIE treatment.

This fabrication of functional FETs using MIMIC demonstrates that soft lithography can be used to fabricate microelectronic devices having satisfactory performance, and that soft lithography can be used for fabrication of microstructures in registration for processes requiring multiple, registered levels. The application of multilayer soft lithography is not limited to microelectronic devices. It should be applicable in many other areas where some registration is needed, such as three-dimensional optical sensors, multilayer MEMS, biosensors, and flat panel displays. The minimum feature size in the system we have used is ~20 μm, but this feature size is determined by the rapid prototyping technique[11] used to make the masters for the elastomeric stamps. We are confident that MIMIC can be easily extended to smaller dimensions with high resolution masters. Combining this with the registration we have achieved here (approximately 12 μm over a 40 mm^2 area) should certainly allow the fabrication of test arrays of transistors and other microelectronic components with minimum feature sizes ≤10 μm.

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