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Fabrication of GaAs/AlGaAs high electron mobility transistors with 250 nm gates using conformal phase shift lithography

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Abstract

This paper establishes the feasibility of soft lithography for fabrication of submicron-scale electronic devices. Near-field conformal phase shift lithography — a representative soft lithographic technique — was used on a broadband exposure tool to fabricate the gate fingers of a high electron mobility transistor (HEMT). The gates of this proof-of-concept device had lengths of 250 nm and widths of 40 μm. The device had a transconductance of 4 mS and a current–voltage response similar to that of a conventional HEMT.

Keywords: Phase shift; Lithography; Microfabrication

A number of unconventional lithographic techniques are being developed in an effort to deliver low-cost means to transfer patterns in the regime, where conventional photolithography is either too expensive or difficult to realize, or inapplicable because of surface topography [1–6]. Soft lithography provides a set of low-cost techniques for transferring patterns onto planar and nonplanar substrates with submicron- to nanometer-scale features over large areas (1–100 cm^2) [2,7]. In recent studies, representative soft lithographic techniques, including micromolding in capillaries (MIMIC) [8–10], microtransfer molding (μTM) [11], and microcontact printing (μCP) [12], have been used for fabrication of electronic components and simple circuits with critical dimensions in the range of 20 μm to 50 μm. These studies have demonstrated the compatibility of soft lithography at this large scale with the processing methods used in conventional device fabrication. The application of soft lithography to submicron-scale electronic device fabrication remained to be established. The purpose of this paper is to demonstrate the application of soft lithography in submicron-scale microelectronic device fabrication through fabrication of a proof-of-concept device incorporating small features — a high electron mobility transistor (HEMT) with gates having lengths of 250 nm— by near-field conformal phase shift lithography using elastomeric stamps.

In this paper, we describe the fabrication of a HEMT on GaAs/AlGaAs heterostructure with submicron-scale gates using a combination of soft lithography and photolithography techniques. The HEMT had an overall dimension of 250 μm × 250 μm. The smallest feature in this HEMT was a pair of gate fingers with lengths of 250 nm and widths of 40 μm. The fabrication of this device involved four levels of pattern transfer. The gate fingers were fabricated by incorporating conformal phase shift lithography with an elastomeric phase mask and photolithography with an amplitude mask. Other noncritical layers in this HEMT, including the mesa, source and drain contacts, and gate contact, were fabricated by photolithography. Room temperature performance of the HEMT displayed the high

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transconductance expected for HEMTs with submicron-scale gates.

Fig. 1 illustrates the schematic HEMT structure. The HEMT was made on a molecular beam epitaxially (MBE)-grown GaAs/AlGaAs heterostructure. Fig. 1(a) is a cross-sectional view of the GaAs/AlGaAs heterostructure, composed of GaAs, $Al_{0.4}Ga_{0.6}As$, and a Si δ-doped layer with a density of 4×10^{12} cm^{-2}. The two-dimensional electron gas (2DEG) was located approximately 430 Å below the surface. The measured 2DEG density and mobility at room temperature were 1.6×10^{12} cm^{-2} and 4×10^{3} cm^2/V s.

Fig. 1(b) illustrates the HEMT layout. The device was fabricated in four steps, with the critical gate fingers patterned using a combination of soft lithography and photolithography and noncritical layers patterned using photolithography. The mesa defined the active region where electrons flowed. It was fabricated in the first step. Photolithography was used to define the mesa pattern: the mesa area was protected by 1 μm of photoresist and the remaining areas were not. The mesa was formed by a wet etch in 10:1 solution of 50% citric acid and 30% hydrogen peroxide. Approximately 500 Å of GaAs/AlGaAs was etched away in the areas that were not protected by photoresist to remove the 2DEG in these areas. The source and drain were Au/Ni/Ge Ohmic contacts. They were fabricated in the second step by photolithography patterning, metal deposition and lift-off. Ohmic contacts were formed by thermal annealing after lift-off. The Cr/Au gate was fabricated in two steps. The pair of gate fingers was

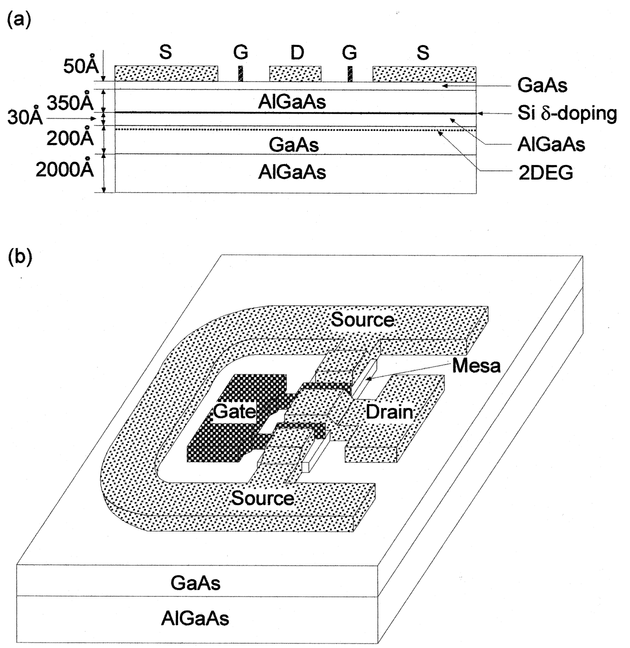

Fig. 1. (a) Schematic cross-sectional view of the HEMT to show the growth profile of the GaAs/AlGaAs heterostructure material. (b) Schematic diagram of the HEMT.

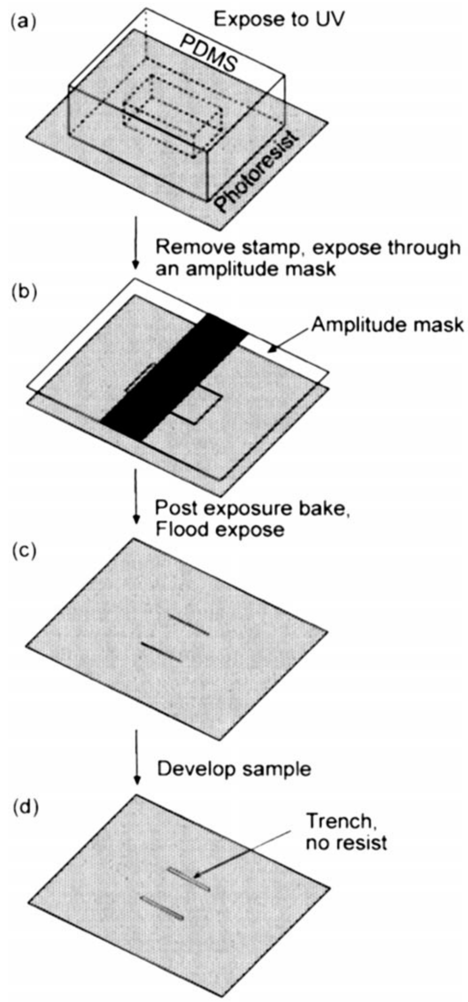

Fig. 2. Schematic illustration of the procedure for fabrication of the two gate fingers using near-field conformal phase shift lithography. (a) Expose the IR photoresist on GaAs/AlGaAs substrate through an elastomeric phase mask with a recessed rectangle pattern. After exposure, the stamp was removed and a latent image of an unexposed open rectangle was formed in the IR resist. (b) Expose the sample through an amplitude mask as shown to expose the left and right lines of the open rectangle and leave the top and bottom lines unexposed. (c) Post-exposure bake followed by flood exposure to reverse the latent image in the IR resist. (d) Develop the sample to form two parallel spaces for gate fingers.

fabricated using conformal phase shift lithography, using a fabrication procedure described in the following paragraph. The gate contact was then fabricated using photolithography patterning followed by metal deposition and lift-off.

Fig. 2 describes the procedure for fabrication of the two parallel gate fingers using near-field conformal phase shift lithography. Phase shift lithography is an optical technique that produces subwavelength features using destructive interference to overcome the feature size limit imposed by optical diffraction [13,14]. Near-field conformal phase shift lithography is based on the same principles of physics. It uses an elastomeric stamp with surface relief structures as

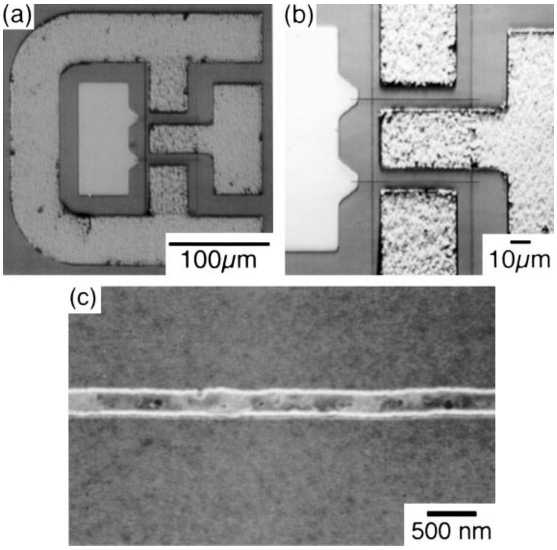

Fig. 3. (a) Photograph of a representative HEMT fabricated using conformal phase shift lithography. (b) Magnified view of the HEMT showing the central active region. (c) SEM micrograph of a section of a gate finger.

a phase mask to produce submicron lines or spaces along the edges of the relief structures [15,16]. The elastomeric stamp used here had a recessed rectangle relief pattern of dimension 42×135 μm (Fig. 2(a)). It was made by casting polydimethylsiloxane (PDMS, Sylgard 184, Dow-Corning, A:B = 1:10) on a master generated by photolithography [17]. The depth of the surface relief of the elastomeric stamp was 0.45 μm and the thickness of the stamp was ~2 μm. The depth of relief was chosen so as to generate destructive interference when exposed to a broadband UV light source with intensity peaks at 365 nm and 405 nm. We used an optical aligner (Karl Suss Model MJB3) for UV exposure and alignment. Its intensity was 10 mW/cm^2 at 405 nm. In the patterning step, we first spin coated the sample with 0.42 μm image reversal (IR) photoresist (AZ 5206-E, Hoeschst Celanese), followed by a soft bake at 90°C for 4 min. We then aligned the elastomeric stamp with the source and drain patterns on the sample using a scheme described previously [8]. The raised regions on the stamp made conformal, atomic-level contact with the substrate. The sample was exposed to UV light through the elastomeric stamp for 5.25 s. This procedure exposed areas other than the edges of the rectangle due to destructive interference, and therefore left a latent image of an unexposed open rectangle in the IR resist. To produce two isolated lines, the wafer, after exposure through the phase mask, was then exposed to the UV light through a second amplitude mask as shown in Fig. 2(b). This second exposure exposed the left and right portion of the rectangle, leaving the center part of the top and the bottom lines unexposed. In Fig. 2(c), 90-s post exposure bake at 115°C, followed by 2-min flood exposure, reversed the latent image in the IR resist. After developing (AZ 422MIF, Hoechst Celenese) for 90 s, two parallel spaces with widths 250 nm were formed on the sample, as shown in Fig. 2(d). The uniformity of the space from sample to sample and over a sample of 5 mm $\times$ 5 mm is within ± 15 nm, measured using an SEM. A Cr/Au deposition and lift-off in acetone followed immediately to form the two gate fingers. Both the width and uniformity of the space were affected by several lithography parameters, including resist thickness, first exposure time, post exposure bake time, flood exposure time, and develop time. Optimum width and uniformity of the space were achieved with the above process parameters.

Fig. 3 shows a representative HEMT fabricated using conformal phase shift lithography. Fig. 3(a) shows a whole device and Fig. 3(b) is a magnified view of the HEMT showing the central structure. The surface roughness of the source and drain was a result of alloying during thermal annealing. The HEMT had an overall dimension of 250 μm $\times$ 250 μm. The mesa was 50 μm wide. The source-to-drain spacing was 10 μm. Fig. 3(c) is an SEM micrograph showing a section of a gate finger. Each finger had a gate length of 250 nm and gate width of 40 μm, leading to a total gate width of 80 μm for the HEMT.

Fig. 4 shows the drain-source current I_{DS} vs. drain-source voltage V_{DS} of the HEMT for a series of gate voltages. It was measured at room temperature in complete darkness. This proof-of-concept device displayed $I_{DS} - V_{DS}$ characteristics typical for this type of HEMTs with submicron-scale gates [18]. The transconductance at $I_{DS} =$ 2 mA was $g_{m0} = 4$ mS. The pinch-off voltage was $V_p =$ 1.75 V. The breakdown voltage was $BV_{DS0} = 10$ V. Higher transconductance can be achieved by reducing the source-to-drain spacing to 2–4 μm, and by making the gate fingers closer to the source to reduce the series resistance. Both require better overlay accuracy.

There is much room for improving the performance of the HEMT, such as optimizing the lithography parameters

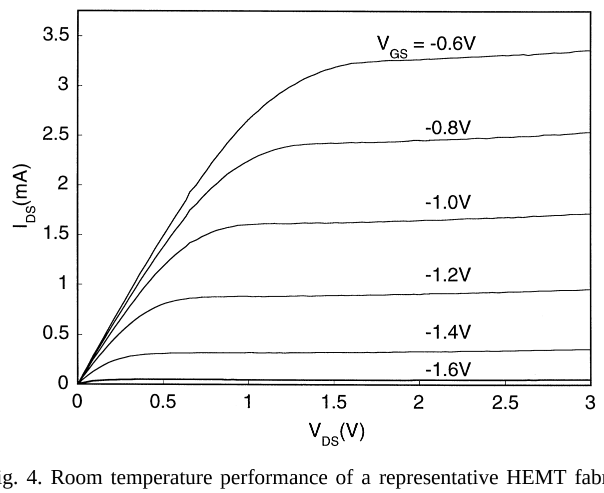

Fig. 4. Room temperature performance of a representative HEMT fabricated using conformal phase shift lithography. The HEMT had a gate length of 250 nm and a total gate width of 80 μm.

discussed earlier to reduce the gate length and improve the uniformity, and utilizing a better HEMT design to achieve higher transconductance. However, we leave this subject to future exploration. It is out of the scope of this paper. The purpose of this paper is to demonstrate the feasibility of soft lithography for fabrication of submicron-scale electronic devices. Even though the performance of this HEMT was not the best, it served the purpose of illustrating how conformal phase shift lithography was used for fabrication of submicron-scale gates of a functional HEMT.

Fabrication of HEMTs with submicron-scale gates demonstrates that incorporation of near-field conformal phase shift lithography — a representative soft lithographic technique — with photolithography provides a simple, low-cost approach to fabricate microelectronic devices with critical dimensions in the submicron regime. A master can be used to make multiple elastomeric phase masks and each elastomeric mask can be used repetitively. Conformal phase shift lithography using elastomeric phase masks will have advantages and disadvantages relative to conventional phase shift lithographies. Because the contact of the elastomeric stamp with the photoresist is soft, the stamp does not damage the resist surface. The conformal contact also insures good destructive interference at the stamp-resist interface, leading to the formation of uniform, narrow lines or spaces. Studies have also shown that lines of 50–250 nm can be achieved using this conformal phase shift lithography [15,16]. In order to fully utilize conformal phase shift lithography for device fabrication, however, distortion and overlay accuracy of the elastomeric masks need to be comparable to that of photolithography. Rogers et al. [19] studied the elastic distortion and overlay of the elastomeric stamps and found that it was possible to control distortion to within 500 nm over a ~ 1 cm^2 area and that errors in overlay accuracy should be the same as for photolithography. Conformal phase shift lithography extends the feasibility of soft lithography for device fabrication down to submicron-scale. As a set of simple, low-cost, versatile pattern transfer techniques suitable for a wide range of feature sizes, soft lithography should have potential applications in simple semiconductor circuits, flat panel display systems, and organic devices.

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Biographies

George M. Whitesides received an AB degree from the Harvard University in 1960 and a PhD degree from the California Institute of Technology (with J.D. Roberts) in 1964. He was a member of the faculty of the Massachusetts Institute of Technology from 1963 to 1982. He joined the Department of Chemistry and Chemical Biology of Harvard University in 1982, and was Department Chairman (1986–1989). He is now Mallinckrodt Professor of Chemistry at Harvard University. Present research interests include biochemistry, surface chemistry, materials science, molecular virology, microfluidics, optics, self-assembly and organic synthesis.

Robert M. Westervelt is Gordon McKay Professor of Applied Physics and Professor of Physics at the Harvard University, and the Director of the Harvard Materials Research Science and Engineering Center. He received his BS Physics degree from the California Institute of Technology in 1971, and his PhD in Physics from the University of California, Berkeley in 1977. He joined the faculty at Harvard in 1979 as an Assistant Professor. His research concerns the physics applications of semiconductor microstructures. He has studied electron interference and quantum chaos in open resonators and in closed stadia, and discovered conductance fluctuations due to chaotic scattering. He has developed new scanned probe microscopy techniques to image electrons inside semiconductor microstructures; he has developed and patented a new type of self-sensing atomic force microscope cantilever incorporating a strain-sensing field-effect transistor. He has used the Coulomb blockade to determine the binding energy of artificial molecules, consisting of two tunnel coupled quantum dots with adjustable coupling. Most recently, he has developed and demonstrated microelectromagnet atoms mirrors made using lithographic techniques. He has served as a panel member for the National Academy of Science, the Office of Naval Research, and the National Science Foundation; as co-chairman of the 1988 Gordon Research Conference on Condensed Matter Physics, as a member of the Board of Editors for Physica D-Nonlinear Phenomena; and as a member of the American Physical Society.

Junmin Hu her BS degree in Physics from the University of Science and Technology of China, P.R. China (USTC), in 1990. She received her AM and PhD in Physics from Harvard University, Cambridge, MA, in 1993 and 1996, respectively. Her doctoral work involved investigation of statistical phenomena in a two-dimensional condensed matter system. From 1996 to 1998, she conducted postdoctoral research in the Department of Chemistry and Chemical Biology at the Harvard University. Her research there concerned fabrication of micro- and nano-electronic devices using soft lithography. She is currently conducting research in lithographic process development for microwave circuits at Hewlett-Packard.

Rex G. Beck received an AB degree in Physics from the Case Western Reserve University in 1992, where he participated in high-temperature superconductivity research with D.E. Farrell. In 1998, he received a PhD degree in Physics from the Harvard University with R.M. Westervelt. His research interests included Nano-Electromechanical systems, low-noise field-effect transistors, and low-temperature atomic force microscopes. Now he studied chemical mechanical polishing as part of the research and development team at Asia et al. Industries' ICMP division.

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Kevin D. Maranowski received a BS degree in Electrical Engineering from Carnegie Mellon University in 1993 and an MS degree in Electrical Engineering from University of California at Santa Barbara in 1995. He is presently pursuing a PhD at UCSB and his current research interests include the growth and characterization of high electron mobility quantum structures.

Arthur C. Gossard received a BA degree in Physics from the Harvard University in 1956 and a PhD from the University of California Berkeley in 1960. He has been a Professor at the University of California Santa Barbara since 1987. He was previously a Distinguished Member of Technical Staff at AT&T Bell Laboratories. His research is centered on the growth of artificially structured materials by molecular beam epitaxy with application to new physics and new optical and electrical devices.