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## Fabrication of Silicon MOSFETs Using Soft Lithography\*\*

By Noo Li Jeon, Junmin Hu, George M. Whitesides,\*  
Martin K. Erhardt, and Ralph G. Nuzzo\*

Microelectronics is based on devices fabricated in silicon, using photolithography to define patterns. As feature sizes approach limits set by diffraction and the transparency of currently available lenses, there is increasing interest in alternative methods for pattern formation: X-ray, e-beam, and extreme UV lithography<sup>[1,2]</sup> are leading candidates, but a range of other techniques—soft lithography,<sup>[3,4]</sup> embossing,<sup>[5]</sup> atom lithography,<sup>[6]</sup> and others—are also contenders for specific technological niches. Soft lithography—a set of techniques for non-photolithographic pattern transfer based on contact printing and polymer molding—is useful in a number of applications to which photolithography is not applicable: examples include patterning non-planar surfaces, forming structures in materials other than photoresists, and patterning large areas in a single process step. Fabrication of transistors requires several distinct steps, in which patterns must be transferred with registration between layers. Key issues in fabrication using soft lithography include minimizing distortion in the elastomeric molds during the pattern transfer steps, and especially carrying out the patterning steps without contaminating the surface of the semiconductor material.

We have recently used soft lithography (micromolding in capillaries, MIMIC) to fabricate high electron mobility transistors (HEMTs) in GaAs/AlGaAs.<sup>[7]</sup> Fabrication of devices in GaAs/AlGaAs involves concerns that are specific to this material, and processes used with it cannot necessarily be generalized to other materials. In this communication, we demonstrate the fabrication of metal-oxide-semiconductor field effect transistors (MOSFETs) using soft lithography as the patterning step. The objective of this work is to illustrate the compatibility of soft lithography with standard silicon processes and to begin to address further issues related to fabrication using soft lithography,

[\*] Prof. G. M. Whitesides, Dr. N. L. Jeon, Dr. J. Hu  
Department of Chemistry and Chemical Biology  
Harvard University  
Cambridge, MA 02138 (USA)

M. K. Erhardt, Prof. R. G. Nuzzo  
Department of Chemistry and  
Frederick Seitz Materials Research Laboratory  
University of Illinois at Urbana-Champaign  
Urbana, IL 61801 (USA)

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especially distortion and registration during pattern transfer. Achieving small feature sizes was not an important objective, and the fabrication of devices with dimensions less than 100 nm is being addressed in separate work in our group.

Figure 1 outlines the fabrication of the p-channel enhanced MOSFET fabricated in this work. The MOSFETs were fabricated on 2 inch (~5 cm) Si wafers. Figure 1a is a cross sectional view of the MOSFET. Figure 1b shows the top view of the device. The device consists of three patterned layers: Al (contact metallization), SiO<sub>2</sub> (gate dielectric), and p<sup>+</sup>-Si (source and drain) regions in n-Si. We fabricated arrays of MOSFETs separately but in parallel using MIMIC and photolithography; the two sets of devices were processed using the same parameters. This strategy made it possible to compare the characteristics of devices generated by these two different classes of technologies. Devices were fabricated in a class 10 000 cleanroom using standard batch diffusion and oxidation furnaces, thermal Al evaporators, and other Si processing equipment.

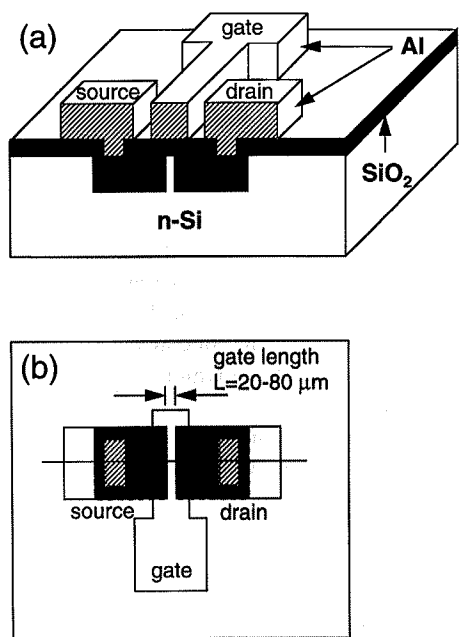


Fig. 1. a) Schematic cross-sectional view that shows the three patterned layers of the p-MOSFET. b) Schematic top view of the device.

Figure 2 summarizes the fabrication steps used in making the p-MOSFETs using MIMIC for pattern transfer. The first MIMIC step patterns the source and drain regions. An elastomeric stamp was prepared by molding a silicone polymer—polydimethylsiloxane (PDMS, Sylgard 184, Dow Corning)—against a patterned photoresist that contained the negative image of the desired pattern.<sup>[8]</sup> The elastomeric mold, with interconnected recessed regions, was then placed in conformal contact with the substrate, and a liquid prepolymer (polyurethane, PU, NOA 73, Norland Products, NJ) was applied at one open end of the mold; the recessed regions between the mold and the substrate filled by

capillarity.<sup>[8]</sup> Exposure to UV light (100 W low-pressure mercury lamp, Boekel Scientific, PA) cured the prepolymer. Removal of the mold left the patterned polyurethane on the substrate.

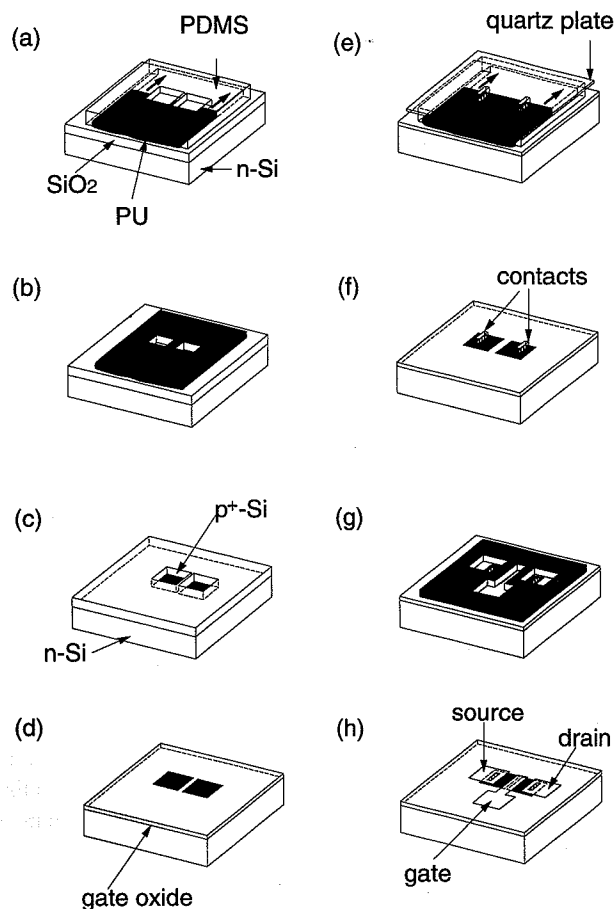


Fig. 2. Schematic illustration of the steps in silicon p-MOSFET fabrication using MIMIC. a) Definition of source and drain regions with the first MIMIC step, using polyurethane (PU) on thermal oxide layer of a n-Si wafer. b) Cure of the PU, removal of the PDMS mold, and etching in buffered HF to remove the thermal oxide selectively. PU patterned by MIMIC was used as an etch mask. c) Removal of PU; after removal, the wafer was placed in a boron diffusion furnace so that exposed regions of n-Si were transformed to p<sup>+</sup>-Si. d) Removal of all oxides, and growth of high-quality gate oxide (350 Å). e) Patterning of contact holes to source and drain regions using second MIMIC step. f) Etching to form contact holes, and removal of PU. g) Definition of regions for Al metallization with third MIMIC step. h) Evaporation of Al on patterned PU and removal by lift-off to leave patterned Al thin film.

The first MIMIC step covered the 1200 Å thermal SiO<sub>2</sub> surface with patterned PU, except for pairs of 200 μm × 200 μm squares (source and drain) separated by 20–80 μm (the gate channel). The total time required for the first MIMIC step was about 20 min: 10 min to fill the channels and an additional 10 min to cure the PU. We used this patterned PU as an etch mask to transfer the pattern into the 1200 Å thermal oxide (SiO<sub>2</sub>) by etching in buffered HF (Fig. 2b). Sonicating the samples in CH<sub>2</sub>Cl<sub>2</sub> for 5–10 min removed the PU from the surface. The patterned wafer was

then loaded into a diffusion furnace with oxidized boron nitride wafers so that the exposed regions of the Si wafer (n-type,  $1 \times 10^{16}$  Sb/cm<sup>3</sup>) were doped with boron to p<sup>+</sup>-type ( $3 \times 10^{19}$  B/cm<sup>3</sup>) (Fig. 2c). All oxides were then removed by etching in buffered HF to expose the bare Si surface. At this point, slight variations in the topology were visible between the doped and undoped regions. A high-quality gate oxide (350 Å) was grown in an oxidation furnace (Fig. 2d). After gate oxidation, the doped and undoped regions could be distinguished by optical microscopy and used in aligning the next layer of the pattern.

The patterning of contacts through the gate oxide for the source and drain regions was carried out using a second registered step of MIMIC (Fig. 2e). The PDMS mold was mounted on a blank quartz plate; the channels in the mold faced the sample. The registration between patterns was carried out on a Karl Suss contact aligner. When the PDMS mold and the sample were aligned, they were brought into contact by raising the sample toward the mold. The sample, together with the quartz plate and the mold between them, was then removed from the aligner. Similar MIMIC and etching procedures (Figs. 2a and 2b) were used to form contacts through the gate oxide onto the p<sup>+</sup>-Si regions (Fig. 2f).

The third MIMIC step defined the regions for Al contact metallization. The patterned PU was formed following the procedure described in Figure 2e. The samples were briefly etched in buffered HF to remove the native oxide at the contacts and were immediately placed in a thermal evaporator for Al deposition. After 2500 Å of Al had been deposited, lift-off (sonicating for 10–15 min in CH<sub>2</sub>Cl<sub>2</sub>) left patterned Al electrodes for source, drain, and gate. Finally, the devices were annealed at 450 °C for 15 min to enhance the contact between Al and Si.

Figure 3 shows a section of the arrays of transistors fabricated by MIMIC and photolithography. The full array consisted of 300 transistors in a 15 mm × 50 mm rectangular pattern. The horizontal and vertical bars prevented sagging of the mold and assisted in making electrical contacts to the substrate during testing. The number of MOSFETs fabricated in an array was determined by the speed with which PU prepolymer filled the channels during MIMIC, and by the area that could be patterned using MIMIC in a reasonable time.

In terms of pattern reproduction, there were no significant differences in the devices patterned by MIMIC and photolithography. The edge roughness (~2 μm) and the resolution (~20 μm) of the structures were similar since the same patterned transparency was used in both cases.<sup>[9]</sup> Slight variations in the feature size of patterns produced by MIMIC were observed from batch to batch due to difficulty in controlling the edge profile/underlayer of filled PU (reactive ion etching was not used to eliminate this underlayer because the equipment was unavailable).

The registration of the features was within 50–100 μm over 50 mm for devices patterned by MIMIC.<sup>[10]</sup> Misalign-

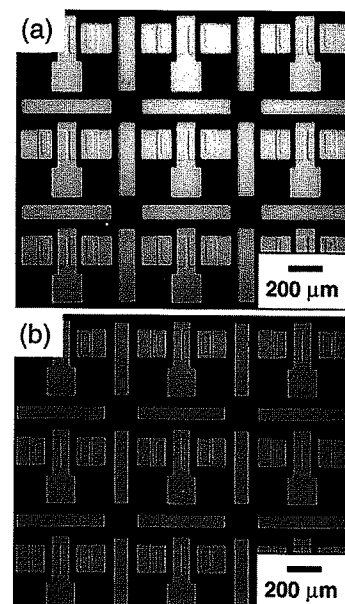


Fig. 3. Micrograph of array of p-MOSFETs (gate length  $L = 20$  μm and width  $W = 200$  μm) fabricated by a) MIMIC and b) photolithography.

ment was more pronounced in regions near the edges of the patterned area. Alignment of features over the entire patterned area was difficult due to the distortion of the elastomeric mold. Using molds that were fabricated from the same batch of PDMS considerably reduced misalignment, but did not eliminate it.<sup>[11]</sup> The overall device yield for the MIMIC process (70 %) was slightly lower than that of the photolithographic process (85 %). This difference was caused primarily by defects generated around the open edges of the pattern where the PU polymer was introduced into the capillaries.

Figure 4 shows representative current–voltage characteristics of the transistors (gate length = 20 μm). All devices, regardless of fabrication technique, had a threshold voltage of  $V_T = -2$  V. The family of current–voltage ( $I_{DS} - V_{DS}$ ) curves confirms the “transistor” nature of the devices. These  $I - V$  curves demonstrate that soft lithography can successfully be used to fabricate functional devices without compromising performance. The electrical properties of the devices tested varied slightly from batch to batch. For example, the transconductances ( $g_m$ ) of transistors with gate lengths of 20 μm ranged from 10 to 20 μS, independent of the fabrication method.

Recently, using a related embossing technique, Guo et al.<sup>[12]</sup> have fabricated MOSFET transistors with 100 nm gate width. In their work, the first layer—that forming the 100 nm gate—was patterned by imprinting a thin poly(methylmethacrylate) (PMMA) layer, and that pattern was transferred into the silicon layer by reactive ion etching (RIE). Two additional levels were subsequently patterned by standard photolithography. Although this work demonstrates the fabrication of electrically functional high-resolution features by imprint lithography, it does not directly

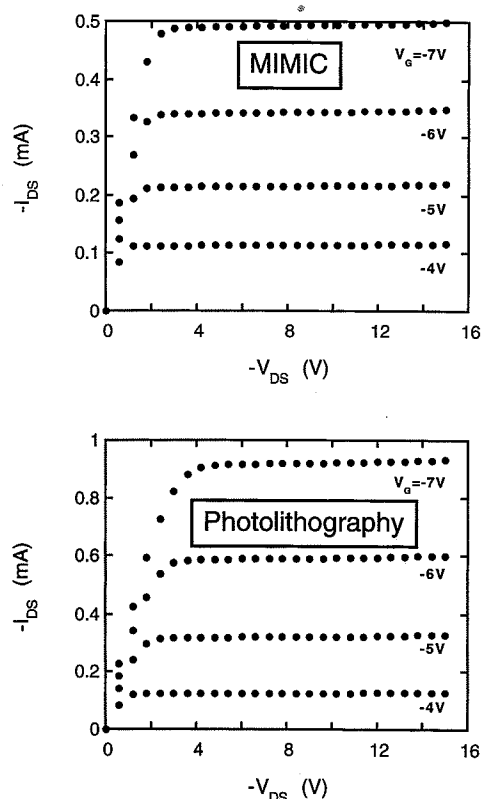


Fig. 4. Current-voltage ( $I_{DS}$ - $V_{DS}$ ) characteristics of p-MOSFETs (gate length  $L = 20 \mu\text{m}$  and width  $W = 200 \mu\text{m}$ ) fabricated by MIMIC (top graph) and photolithography (bottom graph).

address the important issue of registration in multilayer fabrication. The fabrication of transistors demonstrated in this work used soft lithography to pattern three levels in registration, but with large feature sizes. The minimum feature size in the patterns demonstrated in this work ( $20 \mu\text{m}$ ) is relatively large, but is not intrinsic to soft lithography.<sup>[3,4]</sup> We have already demonstrated that the distortion of a pattern can be limited to less than  $1 \mu\text{m}$  over  $\sim 1 \text{cm}$  by using thin elastomeric molds on a rigid backing rather than the thick PDMS molds employed here.<sup>[10]</sup> We believe that in combination with other soft lithographic techniques such as phase-shift lithography<sup>[3,4]</sup> soft lithography can be used to fabricate devices with dimensions less than  $100 \text{nm}$ .

In summary, the fabrication of functional Si MOSFETs demonstrates that MIMIC is compatible with Si fabrication processes. Polymer structures patterned with MIMIC were successfully used as etch masks and lift-off mesas; in particular, they withstood the harsh conditions of etching and lift-off. The electrical properties of the transistors fabricated by MIMIC are similar to those fabricated by photolithography. The fabrication of transistors using multilevel registered processes establishes that the application of MIMIC is not limited to single-level processes.<sup>[7,13]</sup>

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## Influence of Oxygen on Single Molecule Blinking\*\*

By Oliver Panzer, Wolfgang Göhde, Ulrich C. Fischer, Harald Fuchs,\* and Klaus Müllen

In the field of single molecule microscopy the "blinking" phenomenon consisting of discrete on-off transitions in the fluorescence intensity of single dye molecules has recently attracted considerable attention.<sup>[1]</sup> Blinking due to spectral jumps was first observed in single molecule spectroscopy experiments at low temperature.<sup>[2-5]</sup> Spectral jumps have also been observed at room temperature by near-field<sup>[6,7]</sup> and recently by far-field<sup>[8,9]</sup> microscopy. Analyzing single molecule dynamics in systems with many chromophores, blinking was observed within a timescale of seconds.<sup>[10,11]</sup>

Recently, we investigated single terrylenediimide (TDI)<sup>[12]</sup> molecules in a matrix of polyvinylbutyral (PVB) under ambient conditions by means of a combined near-field and confocal microscope.<sup>[13,14]</sup> In the scanned images of many of the molecules dark stripes could be observed, which are due to blinking during the acquisition time of the image. Experiments in which the orientation of the molecules was observed for hours revealed that a rotational

[\*] Prof. H. Fuchs, O. Panzer, W. Göhde, Dr. U. C. Fischer  
Physikalisches Institut, Universität Münster  
Wilhelm-Klemm-Strasse 11, D-48149 Münster (Germany)  
Prof. K. Müllen  
Max-Planck-Institut für Polymerforschung  
Ackermannweg 10, D-55128 Mainz (Germany)

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